NBSIR 77-1301

Interface Standards for Automated Coal Mining Equipment

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Interagency Report

July 1977

Prepared for

U.S. Bureau of Mines
Pittsburgh Mining & Safety Research Center
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U.S. DEPARTMENT OF COMMERCE, Juanita M. Kreps, *Secretary*

Dr. Sidney Harman, *Under Secretary*

Jordan J. Baruch, *Assistant Secretary for Science and Technology*

NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Acting Director*

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INTRODUCTION

This report describes work done at the National Bureau of Standards (NBS) on interface standards applicable to the use of computer control systems with automated mining equipment. The report identifies, analyzes, and recommends interface standards applicable to the modular control system of an Automated Extraction System (AES) being built by the US Bureau of Mines (USBM). The work is intended serve both as a technical guide and as a summary of existing and forthcoming standards applicable to computer control systems. Selected defacto standards are also included for completeness. A complete definition of the scope of work is included in Appendix A.

Since the system configuration of the AES control system has not yet been defined, this report uses several alternative architectures to illustrate various interfaces that may be encountered. The benefits and limitations of the formal and defacto standards which apply to these interfaces are then discussed. In this context, standards are recommended for the supervisory computer - local control computer interfaces and the local control computer - sensor and actuator interfaces. The best use of these standards and important trade-offs are identified and explained.

A critical consideration in the design of any control system is the specification of interface requirements. The use of formal standards at these interfaces simplifies the definition and results in a modular system which is easily maintained and which offers the flexibility of future incremental modifications without total system redesign. It is important to note that the report considers standards only at the interfaces between modular elements of computer based control systems. By adequately standardizing the module interfaces, NBS believes that the Bureau of Mines will be assured of achieving their system performance objectives while leaving vendors free to utilize their creativity and resourcefulness in implementing the functions within any module. The limited use of standards in this way will help both the Bureau of Mines and the vendor develop the most effective control system. This philosophy is general purpose in nature and has application to many complex technical systems developed by the government.

BACKGROUND

One of the strongest motives for developing automation in the mining industry is the need to increase productivity. With many coal-fired thermal power plants planned to fill the capacity shortage created by the delays in placing nuclear power plants into operation and the economic need to convert gas and oil-fired plants to coal, there is a immediate need to increase coal production. However, there has been a decrease in productivity in US underground mines ever since 1969. Productivity has fallen from an all time peak of 15.6 short tons mined per man day in 1969 to 8.5 tons in 1976. This decrease is attributed to several factors including the Federal Coal Mine Health and Safety Act of 1969 and changes in the nature of the work force.

With this goal in mind, the US Bureau of Mines is developing an automated coal extraction system (AES). About 30% of all US bituminous coal production is by room-and-pillar continuous mining methods where electric powered machinery such as the rotary drum continuous miner is capable of mining 5 to 20 tons per minute. Despite this high peak production rate of the continuous mining process, the average rate is only a small fraction as a result of many labor intensive support functions. These additional operations include such tasks as roof bolting, bridge conveyor operations and hauling consumable supplies. The AES is planned to increase productivity by 45% through the automation and integration of several of these functions.

The AES is a 50-ton prototype continuous miner which combines several of these important complex operations so that the mining operation is truly "continuous." For example, it has the capability to both mine and install roof bolts without retreating from the face of the coal seam. At the present time, as noted above, the mining and mandatory roof bolting, (which secures the mine roof) are done by two separate processes which cannot both be accomplished in the same working area simultaneously. The machine is controlled by three personnel who sit in protected cabs of the AES.

The operating environment is harsh for introducing computers and instrumentation. The humidity is 100% and temperatures range from 0 degrees celsius to 60 degrees celsius. Sulfuric acid is constantly forming from the sulfur released from the coal. Methane is also liberated from the coal and, along with coal dust, presents an explosion hazard. Vibration is a problem--in one experiment, an inertial guidance system was unable to withstand the shocks and vibrations. Electrical noise may be a problem since the machine draws considerable electric power for its drive motors. This means that large currents are being switched to and from inductive loads, which can result in severe transient signals.

The typical operation of this device is to approach the coal face on crawlers (tractor treads) and become positioned. Two sets of overhead jacks wedge the AES into the mine and the cutting cycle begins. A normal cutting cycle consists of raising the hydraulic "sumping boom" until the rotary drum cutters touch the roof and then moving the sumping boom forward into the coal seam or "sumping" to the appropriate cut depth, at a rate of 0.2 to 1

inch per second. The boom is then lowered toward the floor in a process called shearing, and the rotary drum cuts the coal from the ceiling to the floor. Although the gathering arms and conveyor may have been in operation during cutting, there will probably be some spillage of coal, and there is also a cusp where the gathering arms come together at the floor behind the cutting drum. Therefore, the sumping boom next draws back to clean the floor. The boom is then raised, and the cycle is repeated. One cycle may take about four minutes. At the present time this sequence is controlled by a drum programmer.

Concurrent with this operation, the roof bolting section of the AES is keeping up with the operations. It installs a row of 4 bolts across the roof on 1.2 meter centers. It is planned that the forward mining section be extended from the roof-bolting section in such a way that the roof is always supported by the AES itself. After a row of roof bolts are inserted, the roof bolting section of the AES can move forward.

The AES operates in conjunction with a conveyor haulage system which can extend 30 meters to collect the coal disposed at the tail boom conveyor of the AES and transport it to larger conveyors which take the coal to the surface. The opposite end of the conveyor system will be an important part of the AES's guidance system. The conveyor system is composed of three sections which can extend and contract and are joined at their ends to each other. A "vector" guidance system is planned which will measure their length and angle with respect to each other as well as to the fixed end, and thus locate the AES to one part in 100 in the X-Y plane. In this manner the AES knows its location relative to the fixed point.

Thus, it is possible to identify four distinct operations of the AES: the cutting cycle, the roof support cycle, the roof bolting cycle, and the guidance function. Presently, the control systems involved in these operations are either of the drum programmer type or are manual. USBM anticipates the development of a computer based AES control system to automate and integrate these operations. This report investigates the use of interface standards in such a development.

INTERFACE STANDARDS

In the development of a computer based control system for the AES there will be a wide variety of interfaces to define. An interface in a data communications system is a common boundary which enables two units to exchange information and control each other's operation. There are many different aspects to an interface, including hardware, operating procedures, and software. Communications interfaces are specified at several, generally independent, levels. Each of these levels specifies some additional aspect of the total operation.

To unravel the mysteries of a communications interface, it's best to consider a simple (but not too simple) example , such as the interface between a synchronous terminal -- a remote batch entry station -- and a modem.

First of all is the mechanical aspect of the interface. This specifies the way in which the two devices are actually connected mechanically. It includes the number of wires and the dimensions of the physical connectors (generally a male and female connector are specified) in which the wires terminate. For example, a 25-pin connector is currently in widespread use for computer-communications interfaces.

The electrical aspect of the interface specifies the voltage levels and duration (or for some interface specifications, the current flow) to be used for signaling on the various leads. The basic capability provided by adherence to the standards at this level is the transfer of data bits across the interface.

The way in which the data bits are interpreted is the subject of the procedural aspect of the interface. This portion of the interface specifies how the data bits and/or characters are grouped into fields for the purposes of signaling and data transfer. Specifications at this level determine the legal sequences of communications control characters, or the legal contents of various fields, or the valid commands and responses in controlling data flow. The same basic set of control characters or fields may be used in a variety of different ways according to the procedural specifications.

The final aspect of communications interfaces are the protocols which define the conventions used at various levels for initiating or terminating calls, for data link control and in general to govern the actual flow of data across the interface.

It is probably the protocol that is most difficult to understand. Protocol can be defined as "a formal set of conventions governing the format and relative timing of data exchange between two communicating processes." As you might expect, each phrase in the definition is significant and needs explaining. A simple example might be the best way to do that.

When you call someone on the telephone, there is a protocol that both parties must follow to establish and maintain the conversation and to convey information. Knowledge of the phone number and how to dial it is part of the protocol, as is the called party's recognition of the bell as a signal to pick up the receiver. The party then says "Hello" or something to that effect. When this happens, you reply with your identity, and the main business of the conversation begins. If not, you inquire for the right party, receive an acknowledgement , and the conversation begins.

During the conversation both parties speak the same language, one at a time, pausing at the appropriate time for the other to reply. If there is too long a pause before a reply, the one who last spoke may inquire if the other is still there. Finally, you finish your conversation, say goodby, and hang up. All these procedures and conventions are part of the protocol necessary to use the telephone.

Note that the procedure for the call may be broken into several parts with a separate set of conventions for each part. First there is a call establishment phase, which for telephone usage includes dialing, recognizing the ring, answering, and identifying both calling and called parties. There are two time-outs included in the protocol for this phase: 1) if the phone is not answered after a certain number of rings, you will hang up; and 2) after the receiver is lifted you will wait a certain period of time for an answer before saying "Hello?" The person answering the phone will likewise wait a short period of time after saying "Hello" for his reply.

After the call establishment phase comes the data transfer phase: the parties talk to each other and transact their business. The mechanics of this data transfer are basically two-way alternate, commonly called half-duplex, in which either party but not both can speak. There is a time-out period whenever the speaker pauses, after which he will inquire if the other party is still there. (In computer communications these inquiries are commonly called handshaking.) If there is no reply to an inquiry, it may be repeated a number of times, after which the conversation may end.

Finally, the business of the conversation is completed, and each speaker indicates to the other the intention to terminate. Only after each party agrees and the agreement is acknowledged does the conversation end. Each party then closes down the connection (hangs up).

Looking back at the definition of protocol now, "A formal set of conventions" means that there are a set of rules that both sender and recipient understand and agree to use. (For computers it is critical that the rules be well defined and complete.) Message format applies more directly to data communications than to human speech, though even spoken English has its own format. "Relative timing" is quite important, for it determines who transmits and who receives at a given time, and also specifies time-outs. The term "communicating processes" generalizes the notion of sender and receiver; in data communications, it emphasizes that communications may occur between different types of equipment.

There are then four major aspects of an interface:

Mechanical
Electrical
Procedural
Protocol

Of these, the first three are generally handled by hardware while the last is often implemented in software. In data communications, protocols govern the information interchange between two units, one or both of which may be a program in a computer. Coupled with the mechanical, electrical and procedural aspects, they completely define the interface. Standards already exist in each of these areas. Some are more comprehensive than others in that they address several or all of the elements of the interface at once. These points should be kept in mind as we define a proper role for interface standards in the development of the AES control system.

STRATEGIES FOR MODULAR CONTROL

There are five basic components to a control system. These include the actuators, sensors, controller, man-machine interfaces, and the process or activity itself. The actuators are those elements which can effect a change in the operating variables of the process, and include such devices as motors, heaters and valves. Sensors measure the changes in the operating variables and include such devices as thermocouples, pressure transducers, and proximity switches. The controller processes the signals from the sensors and issues the required commands to the actuators to maintain a programmed course of action. The man-machine interfaces permit people to interact with the system to make limit adjustments and to monitor the system's operation. The last component is the activity itself which is being controlled. Before considering architectures for the control system, it is useful to examine three of these elements in more detail: the actuators, the sensors and the controller.

Sensors and Actuators

In general, sensors and actuators are needed by every control system to measure important operating variables and to cause changes in the activity. Both mechanical and electronic types of each component may be used depending on the control system. The AES electronic control system requires sensors and actuators which communicate by means of voltages or currents with the controller. Considering the computer based oontroller planned for the AES, the sensor input must at some point be digitally coded for processing. If the sensors are transmitting analog voltages, the computer will require a peripheral analog-to-digital converter for transforming those signals into the proper form. If there are digital signals or a string of digital signals, other types of peripherals will be necessary to process the information.

The sensors themselves may produce either digital or analog information. A sensor with digital information may simply tell the control system of an on-off condition in the process such as exceeding a position limit. On the other hand, analog inputs from sensors are often required to report the continuous changing of an important variable.

There is a corresponding problem with the computer outputs to various actuators. Digital signals can be used to control some actuators directly such as on-off valves. In other cases analog continuous control of an actuator is required. Here a digital -to-analog converter will be necessary. The AES control system may include a mix of analog and digital signals.

Digital signals, as compared to analog signals, are less prone to error. This is because the range of voltage levels which the control system considers "on" or "off" can be wide giving less susceptibility to electrical noise and attenuation. For this reason, some sensors are now available which include encoding electronics to convert the analog output of the sensor to a digital pattern which can be transmitted over a distance to the

control system. Digital pyrometers and pressure transducers are some of those which are available with this feature. It is important to note in these particular cases that the information at the sensor is analog but it is transmitted digitally to the controller. Standard codes and nardware interfaces including RS 232-C and digital parallel interfaces are readily available to operate in this mode and are included in this report.

The AES will have a variety of actuators and sensors. A study entitled "Data Flow Requirements for Remote Supervisory Control to Continuous Mining Machine" predicted that 88 sensors and 23 actuators would be necessary to operate a comparable mining machine. Selecting the proper sensor-to-control system and actuator-to-control system communications interfaces are very important. This report will describe and evaluate several alternatives for these interfaces.

Controller

In its simplest form a controller compares the input command against sensor data from the process or activity. Where the two do not agree, an error signal is computed and is applied to the actuator in such a way as to reduce the error to zero. Three components then form what is called a "control loop": the sensors, actuators, and the controller. A control system may consist of one or more of these control loops while complex control systems may include a hierarchy of control loops. First there are local control loops which directly connect the controller to the actuators and sensors. Interfaces here will be referred to as "local instrumentation" interfaces in this report. Other control loops exist at higher supervisory levels in the hierarchy and are used for the overall control of the system. Interfaces at this level will be referred to as "system control" interfaces.

Control System Architectures

The choice of interface standards is governed by two factors critical to organizing a modular control system: the functional organization (what the modules will do), and the communications network (how the modules will comunicate). The functional organization includes the jobs to be done and considers both the degree of supervision required by each module and the degree of supervision exerted by each module. The communications network is concerned with how the modules exchange information. The two are not independent since the nature of the communications interfaces are determined by the functional organization of the system.

Functional Organization

The most common process control organization is the hierarchical organization. As applied to the AES, it could be shown as Figure 1 . The lowest level is occupied by the function controller that directly regulates a single activity on the mining machine, such as the cutting cycle. This lowest level controller carries out sequential operations and interacts with a variety of sensors and actuators. Interfaces at this level are termed "local instrumentation" interfaces. The next higher level is responsible for coordinating several related activities for scheduling operations, and for optimizing the machine performance. This is the system control interface.

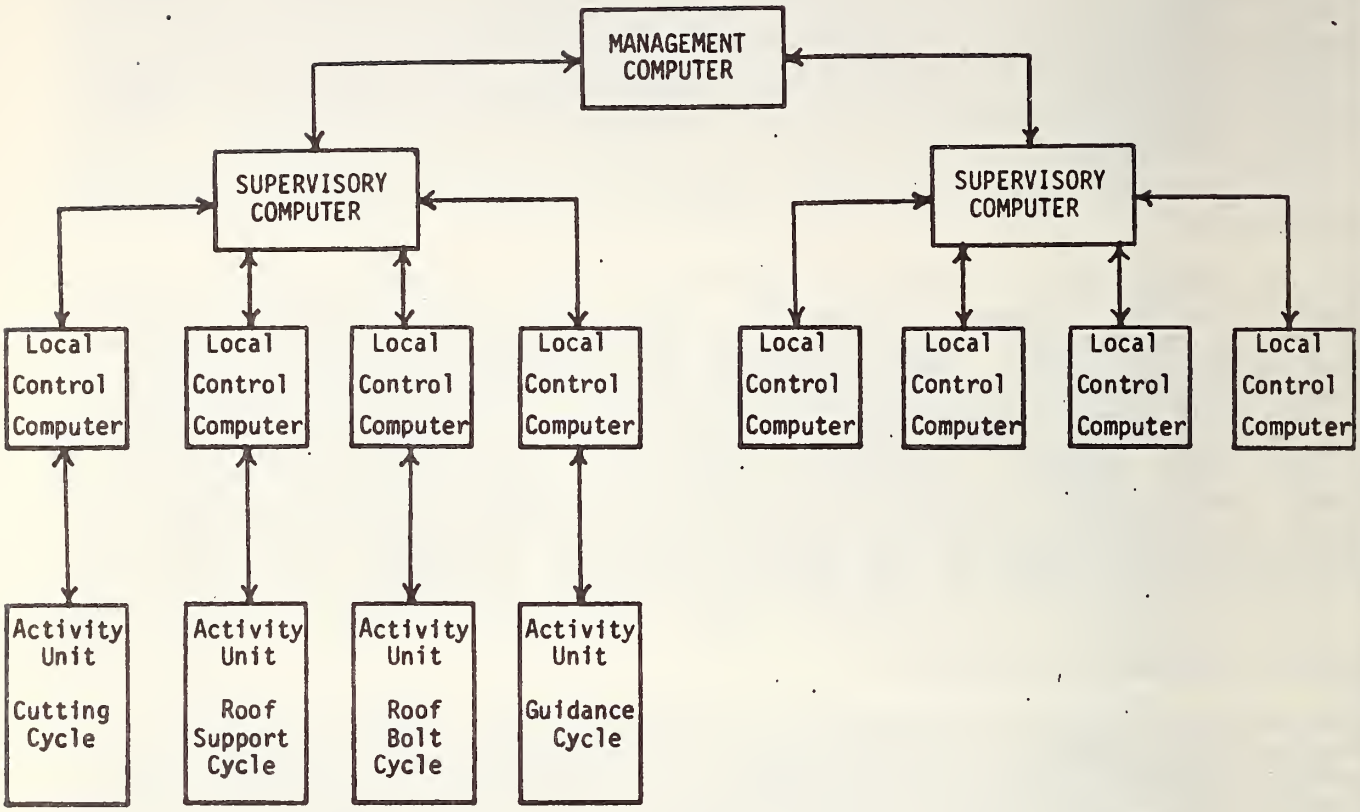

MANAGEMENT COMPUTER
SUPERVISORY COMPUTER
SUPERVISORY COMPUTER
Local Control Computer
Local Control Computer
Local Control Computer
Local Control Computer
Local Control Computer
Local Control Computer
Local Control Computer
Local Control Computer
Activity Unit Cutting Cycle
Activity Unit Roof Support Cycle
Activity Unit Roof Bolt Cycle
Activity Unit Guidance Cycle

Figure 1

At the top level is the corporate control computer. While not presently a part of the AES, this level in the hierarchy could be added to control two or more AES machines and to make current information about mining operations available to management. Additionally, with these interfaces it would be possible to provide remote diagnosis for AES maintenance from a central site. While this level in the hierarchy will not be considered in this report, it should be pointed out that specifications for the interfaces at this level are well developed being either in the draft stage or already approved as formal standards. USBM may wish at some future time to investigate this additional opportunity.

The hierarchical organization represents an advanced automation system since it is concerned not only with the physical control of the activities but also with its management (the gathering and application of both machine activity and business information for decision-making). The operations at the lowest level (of regulating the activities and watching for system failures) are the simplest and must be done most frequently. The optimizing and scheduling tasks at the higher levels are much more complex but they must be done less frequently. This consideration will be important for deciding on a network architecture and for choosing the appropriate standards for the various interfaces.

Communications Network

The communications network for the AES modular control system is a critical component. Its architecture must be chosen not only on the basis of performance but also on reliability, maintainability, flexibility, and cost. There are three common types of architecture to consider for local control applications (as distinct from general communications networks.)

The central or "star" structure
The distributed or "bus" structure
The "ring" structure.

All of these structures assume that there are computers in the system with resources to be each other to best meet the objectives of the system. These computers are referred to as "nodes" in the communications network, and the architecture determines how the nodes communicate within the network. For the AES, the objective of the network must be to effectively control the hardware involved in the coal extraction process. While the hardware configuration is well known, the architecture of the AES control system has yet to be detailed. For this reason it is difficult to make recommendations for appropriate interface standards. However, by examining the three architectures mentioned and analyzing the applicability of various interface standards to these architectures, much can be learned for use with the AES. The next two sections provide this analysis first for the local instrumentation interfaces and secondly for the system control level interfaces.

STANDARDS FOR THE LOCAL INSTRUMENTATION INTERFACE

The specifications for the AES control system describe four functions which will be automated. These include the cutting cycle, roof support cycle, roof bolting cycle, and guidance. The modular nature of the function being automated clearly points to a similar organization of the local control system. There are many advantages to designing modularity into a complex control system such as this, including the ease of adding or changing subsystems and the ability to accomodate design changes. Standards for the many local instrumentation interfaces here are well defined. A designer is able to utilize existing standards for the mechanical, electrical and procedural aspects of the interface. Alternatively, he may choose one of the complete instrumentation package standards which encompass all of these aspects. This section will present a view of the proper application of interface standards at the instrumentation level. It will show where a standard is useful and the benefits and limitations of its selection. Summary data sheets on each of the standards mentioned are included at the end of the section, and complete technical descriptions are given in Appendix B.

Figure 2 serves to illustrate the applicability of interface standards to a modular functional controller. Four such controllers are envisioned for the AES with each being implemented via a microcomputer or other programmable logic. The module is seen as a self-sufficient activity which, when initiated with the necessary parameters, can carry out its task without communication with other modules.

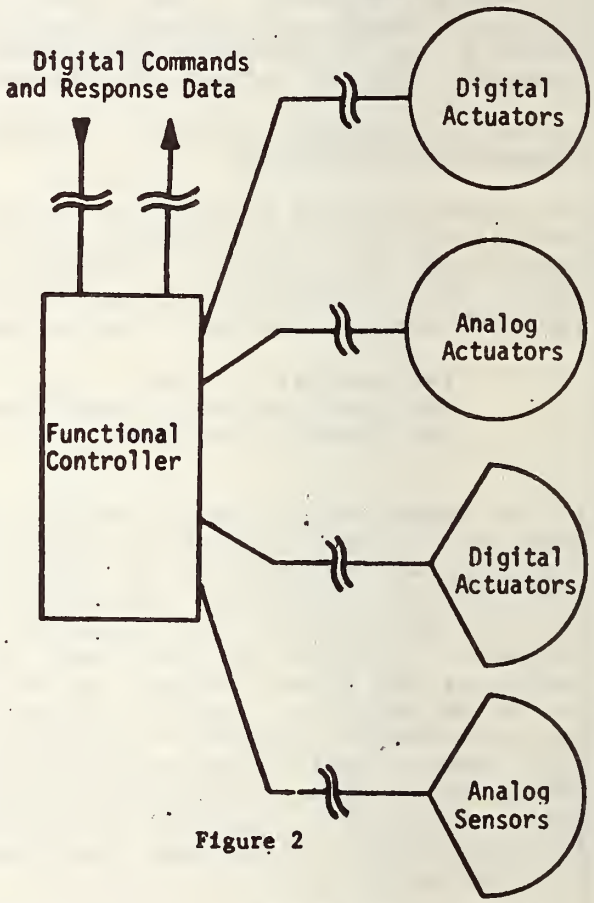


Figure 2

Operations within the module are performed quite frequently with the remote actuators and sensors communicating with the local microcomputer via voltages, or currents. The actual form of that communication can be classified first as being analog or digital. Other considerations include whether the communication is bidirectional, the speed at which the information must be transmitted, its volume, and the degree of error which can be tolerated. The exact choice of standards depends upon all of these factors.

Similarly, sensors and actuators can be classified as analog or digital. Shaft encoders and solenoid valves are primarily digital while motors and potentiometers are usually analog in nature.

Analog Interfaces

For analog sensors and actuators the concern is how and where to make the conversion to interface with the digital controller. Incoming analog signals must be digitized either at the sensor or at the local control computer. Likewise, outgoing control commands must go through a corresponding conversion from digital to analog for some actuators. Several options for transmitting sensory data to the local control computer will be discussed next. It should be noted that the same transmission considerations apply to data being sent to the actuators.

When analog signals are sent directly to an A/D converter at the local control computer as in figure 3, the local instrumentation interface is analog. While no formal standards exist, analog voltages generally are between the limits of -5 to +5, or -1 to +1, or 0 to 10 volts. Communication takes place over a two wire cable at a maximum speed determined by the computer and the A/D or D/A converter. For microcomputers this rate is typically no more than 5000 samples per second.

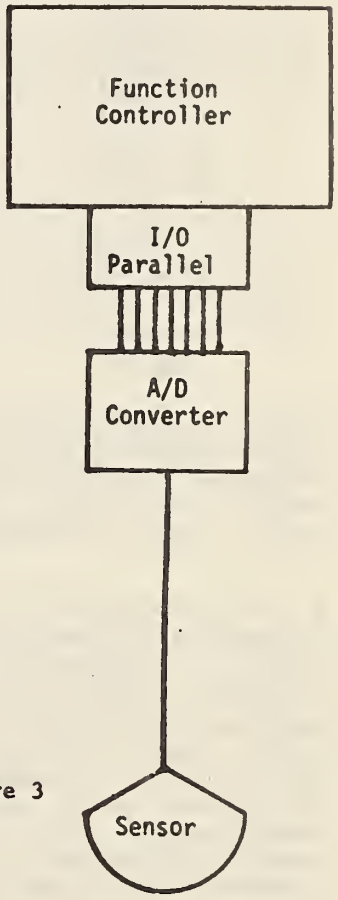


Figure 3

The main disadvantages of this configuration are the electrical noise picked up by the wires and the attenuation in the cable which affect the quality of the analog signal. Generally the A/D range is fixed. Therefore, an 8 bit converter with an analog input of zero to 10 volts would have a resolution of about 40 millivolts. If the noise and attenuation are much less than this, there should be no problems so long as 8 bit accuracy is all that is required.

Digital Interfaces

With analog transmission of signals, the disadvantages are more apparent with sensors than with actuators since sensors usually involve high impedence circuits. In this situation, and in the potentially harsh electrical environment of the AES, a better method would be to digitize as close to the origin of the signal as possible. In this configuration the maximum speed of digitizing may be reduced because of longer settling times in the lines, but this limitation is more than offset by the ease of extracting the digital signals from background noise without loss of information. Here the local instrumentation interface is digital, and several formal and defacto standards are applicable.

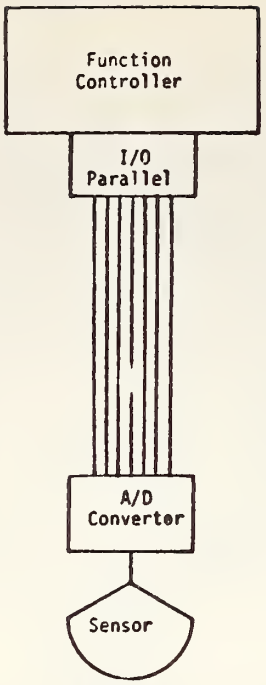


Figure 4

Two basic options for digital transmission are possible, parallel or serial. Figure 4 considers the parallel case. Transmission here is termed bit parallel, byte serial. Each byte is a finite number of bits, often 4, 8 or 16. Bytes are coded in a certain convention such as Binary Coded Decimal (BCD) or American Standard Code for Information Interchange (ASCII). The BCD parallel interface is a defacto standard found commonly with thumbwheel switches and digital readout devices. The Electronic Industries Association (EIA) has published RS-408 originally to define the bit parallel, byte serial interface between a paper tape reader and the controller of a numerically controlled machine tool. RS-408 is capable of transmitting any 7 or 8 bit code like ASCII and certainly may be relevant to the AES project. Electrical specifications with either BCD or RS-408 generally conform to the defacto TTL convention of zero and 5 volts.

A minor disadvantage of the digital parallel interface is the number of wires associated with each sensor. A multi-wire cable is necessary and is expensive for long runs. For instance, to transmit two digits in BCD format would require at least 11 lines (8 for data, 2 for control and one common wire). Also transmission in bit parallel form is generally unidirectional.

A great reduction in the number of wires can be made by transmitting the data serially as shown in Figure 5. LSI circuits are available commercially which can convert parallel signals, such as the A/D converter output into serial for transmission over a single pair of wires. The message rate is of course much slower than with parallel transmission. Undoubtably the most widely used interface standard for serial transmission of digital data in the United States is the RS 232-C. This standard specifies not only the electrical and functional characteristics of the interface but the mechanical plug connection as well. With RS 232-C a wide range of options are available to the user. For instance, communication can be one way (simplex), two way (duplex) or two way simultaneous (full duplex). Although this latter form requires a minimum of four wires, it allows considerable flexibility in communicating with an intelligent device such as a "smart sensor" like the Coal Interface Detector.

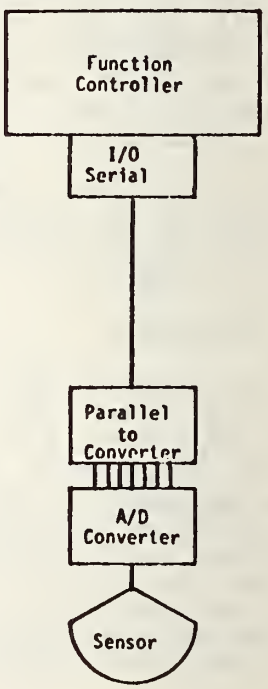


Figure 5

If a functional controller can communicate in this fashion with each of its sensors and actuators, it can also perform automatic calibration and diagnostic checking. Maintenance for the AES as a whole would be simplified, and productivity objectives could be more easily achieved.

Serial transmission data rates are expressed in bits per second and can range up to 20,000 bps with RS 232-C over 12 meter cable lengths. Keeping in mind this is bit serial, transmission in this mode is often too slow for some applications. A successor to RS 232-C, designated as EIA standard RS-449, will enable serial transmission at rates up to 10 million bps and distances up to 1000 meters.

Discussion of serial bit transmission would not be complete without mention of the 20 ma current loop interface. Bits are represented by the flow of current in the line as contrasted to RS 232-C which uses voltage levels. The current loop interface is very widely used. Although not documented as a formal standard, it is nevertheless quite useful for low speed, asynchronous transmission. It has good noise immunity and performs over long distances of simple twisted pair lines.

Table 1 summarizes the characteristics, standards, benefits and limitations of the several options discussed for the AES local instrumentation interfaces to actuators and sensors.

Table 1 - Comparison of Data Transmission Methods

Transmission Method	Available Standards	Maximum Distance	Maximum Speed	Noise Immunity	Wire Volume
Analog	none	30 m	5 K hertz	poor	low
Digital Parallel	BCD or TTL	15	1 K char/sec	fair	high
	RS - 408	10	10 K char/sec	fair	high
Digital Serial	RS 232-C	12	20 K bits/sec	good	low
	RS 449	1000	10 M bits/sec	good	low
	20 MA loop	1000	1 K bits/sec	excel	low

Summary Data Sheets

The following pages list summary data on the various standards mentioned in this section on the Local Instrumentation Interface. Included here are the following:

EIA RS 232-C
EIA RS 408
EIA RS 449
ANSI x3.16 (ASCII Serial)
ANSI x3.25 (ASCII Parallel)
Parallel Interface (TTL)
20 MA Current Loop

1. DESIGNATION: EIA RS 232-C, August 1969

2. TITLE: Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange, August 1969

3. MAINTENANCE AUTHORITY: Electronic Industries Association, Subcommittee TR-30.2

4. SCOPE: Hardware Standard. "This standard is applicable to the interconnection of data terminal equipment (DTE) and data communication equipment (DCE) employing serial binary data interchange." It defines: (1) electrical signal characteristics, (2) interface mechanical characterstics, (3) functional description of interchange circuits, (4) standard interfaces for selected communication system configurations.

5. RELATIONSHIP TO OTHER STANDARDS: EIA RS-334 (ANSI X3.24-1968) Signal quality for EIA RS 232-C interface EIA RS-422 and EIA RS-423, April 1975 (revised electrical signal characteristics) EIA RS-449.

6. COMPETITIVE STANDARDS: CCITT V.24 (functional) and V.28 or V.31 for electrical characteristics. CCITT X.21 corresponding interface for public data (in contrast to public telephone) networks.

7. STANDARDIZATION STATUS: RS 232, May 1960; RS 232-A, October 1963; RS 232-B, October 1965. RS 232-C is expected to be gradually (ten years) replaced by EIA RS-449.

8. IMPLEMENTATION STATUS: Commercially, RS 232-C has enjoyed universal acceptance as the data terminal-to-modem de facto interface. Although MIL STD 188C prescribes RS 232-C functions, it employs different (lower voltage and lower impedance) electrical characteristics, primarily for security and privacy purposes.

9. KNOWN MANUFACTURING USES: RS 232-C is primarily a communications (serial) interface specification.

10. KNOWN SOURCES OF INFORMATION: Mr. A.M. Wilson, Electronic Industries Association, 2001 Eye Street, NW, Washington, D.C. 20006, (202)659-2200.

11. PROBABLE SOURCES OF INFORMATION: Mr. George E. Clark, National Bureau of Standards, Building 225, Room B210, Washington, D.C., 20234, (301)921-3723.

12. BIBLIOGRAPHY: EIA RS 232-C, August 1969

13. COMMENTS: Equipment conforming to RS 232-C will gradually be replaced with that conforming to RS-422 and 423 (employing integrated circuit components) that will also operate over much greater distances (up to 1200 meters) and at much higher speeds (up to 10 mega bits/sec.). (Note that RS 232-C is constrained to 20 kilobits/sec and 12 meters).

1. DESIGNATION: EIA RS-408

2. TITLE: Interface Between Numerical Control Equipment and Data Terminal Equipment Employing Parallel Binary Data Interchange

3. MAINTENANCE AUTHORITY: EIA EI-31

4. SCOPE: Hardware Standard. This standard applies to the interconnection of data terminal equipment and numerical control equipment at the tape reader interface. It provides electrical signal characteristics, interface mechanical characteristics, and a functional description of the interface.

5. RELATIONSHIP TO OTHER STANDARDS: This standard is for parallel-by-bit, serial-by-byte data, such as that generated by a perforated tape reader.

6. COMPETITIVE STANDRDS: IEEE Standard 488-1975

7. STANDARDIZATION STATUS: Approved by EIA in March 1973

8. IMPLEMENTATION STATUE: Widely implemented in numerical control equipment.

9. KNOWN MANUFACTURING USES: Used in machines employing numerical control.

10. KNOWN SOURCES OF INFORMATION: Mr. A.M. Wilson, EIA, (202)659-2200; Dr. John Evans, NBS, (3101)921-2381.

11. PROBABLE SOURCES OF INFORMATION: NMTBA

12. BIBLIOGRAPHY: EIA RS-408, March 1973

13. COMMENTS: The data terminal equipment (DTE) typically includes a serial-to-parallel converter. This standard is employed on the parallel-by-bit side of the DTE. Other standards, such as EIA RS 232-C, apply at the serial-by-bit side of the DTE.

1. DESIGNATION: RS-449 / Proposed Federal Standard 1031

2. TITLE: Functional and Mechanical Interface Between Data Terminal Equipment and Data Communication Equipment

3. MAINTENANCE AUTHORITY: Electronic Industries Association Subcommittee RS-30.2.1

4. SCOPE: RS-449, together with EIA RS-422 and RS-423, is intended to supersede EIA RS 232-C.

5. RELATIONSHIP TO OTHER STANDARDS: This Standard, together with EIA Standard RS-423, is intended to gradually replace EIA Standard RS 232-C as the specification for the nonengineered interface between data terminal equipment (DTE) and data communication equipment (DCE) employing serial binary data interchange. With a few additional provisions for interoperability, equipment conforming to this standard can interoperate with equipment designed to RS 232-C.

6. COMPETITIVE STANDARDS: RS 232-C

7. STANDARDIZATION STATUS: Adopted by EIA

8. IMPLEMENTATION STATUS: None

9. KNOWN MANUFACTURING USES: For digital serial communication links.

10. KNOWN SOURCES OF INFORMATION: Mr. A. M. Wilson, Electronic Industries Association (202) 659-2200

11. PROBABLE SOURCES OF INFORMATION: Mr. George E. Clark, NBS, (301) 921-3723

12. BIBLIOGRAPHY: EIA RS-449

13. COMMENTS: Commonly referred to as RS-XYZ while under development. A notice of an earlier version (EIA SP-1194) of this standard as a proposed Federal Standard (1031) and a proposed FIPS PUB appeared in the Federal Register on December 5, 1975, page 56938.

1. DESIGNATION: FIPS PUB 17-1971/ANSI X3.16-1966

2. TITLE: Character Structure and Character Parity Sense for Serial-by-Bit Data Communication in ASCII (FIPS PUB 1/ANSI X3.4-1968)

3. SCOPE: Hardware Standard. This standard specifies the character structure and sense of character parity for serial-by-bit, serial-by-character synchronous and asynchronous data communication in ASCII (FIPS PUB 1, ANSIC X3.4-1968). This standard applies to general information interchange at the interface between data processing terminal equipment and the data communication equipment.

4. RELATIONSHIP TO OTHER STANDARDS: This standard is an implementation of the 7-bit code of ASCII (FIPS PUB 1/ANSI X3.4-1968). It is used at interfaces such as EIA RS 232-C. The companion standard FIPS PUB 18/ANSI X3.25-1968 is for character structures using parallel-by-bit data communication. Subsets, such as EIA RS-358, can use the structure of this standard.

5. COMPETITIVE STANDARDS: Proprietary structures for communicating non-ASCII codes, such as 6-bit Teletypesetter or 8-bit EBCDIC

6. STANDARDIZATION STATUS: The ANSI standard X3.16 was approved on August 19, 1966; FIPS PUB 17, adopting in its entirety that ANSI standard, was approved on October 1, 1971.

7. IMPLEMENTATION STATUS: Widely implemented in communication systems and ADP terminal devices.

8. KNOWN MANUFACTURING USES:

9. KNOWN SOURCES OF INFORMATION: Mr. John L. Little, NBS, (301)921-3723; Mr. George E. Clark, NBS, (301)921-3723.

10. PROBABLE SOURCES OF INFORMATION: Teletype Corporation

11. BIBLIOGRAPHY: FIPS PUB 17-1971/ANSI X3.16-1966

12. COMMENTS: This standard specifies odd parity for synchronous data communication and even parity for asynchronous data communication. It does not specify the bit sequence, which is given in FIPS PUB 16/ANSI X3.15-1966.

1. DESIGNATION: FIPS PUB 18-1971/ANSI X3.25-1968

2. TITLE: Character Structure and Character Parity Sense for Parallel-by-Bit Data Communication in ASCII (FIPS PUB 1/ANSI X3.25-1968)

3. MAINTENANCE AUTHORITY: NBS/ANSI X3S33

4. SCOPE: Hardware Standard. This standard specifies the character structure and sense of character parity for parallel-by-bit, serial-by-character, data communication in ASCII (FIPS PUB 1/ANSI X3.4-1968). This standard applies to general information interchange at the interface between data processing terminal equipment and data communication equipment.

5. RELATIONSHIP TO OTHER STANDARDS: This standard is an implementation of the 7-bit code for ASCII (FIPS PUB 1/ANSI X3.4-1968). It is used at parallel-by-bit interfaces, such as EIA RS-408. The companion standard FIPS PUB 17/ANSI X3.16-1966 is for character structures using serial-by-bit data communication. Subsets, such as EIA RS-358 can use the structure of this standard.

6. COMPETITIVE STANDARDS: Proprietary incompatible structures for communicating non-ASCII codes, such as 8-bit EBCDIC.

7. STANDARDIZATION STATUS: The ANSI standard X3.25 was approved on September 27, 1968; FIPS PUB 18, adopting in its entirety that ANSI standard, was approved on October 1, 1971.

8. IMPLEMENTATION STATUS: Implemented in most parallel-by-bit data communication devices.

9. KNOWN MANUFACTURING USES:

10. KNOWN SOURCES OF INFORMAION: Mr. George E. Clark, NBS, (301)921-3723; Mr. John L. Little, NBS, (301)921-3723.

11. PROBABLE SOURCES OF INFORMATION:

12. BIBLIOGRAPHY: FIPS PUB 18-1971, ANSI X3.25-1968

13. COMMENTS: This standard specifies an 8-bit character structure including the 7 bits of ASCII and an odd parity bit where the character timing is not separately signaled. Where the character timing is on a separate timing channel, the priority sense is even.

1. DESIGNATION: Parallel Interface

2. TITLE: Parallel Interface (TTL)

3. MAINTENANCE AUTHORITY: Not a formal standard.

4. SCOPE: De facto hardware standard. This standard defines requirements for bit parallel transmission on a multicondictor cable. It only specifies the electrical format to be employed.

5. RELATIONSHIPS TO OTHER STANDARDS: TTL: The integrated circuits most commonly used in logic design are based on transistor/transistor logic (TTL), which may be regarded as the industry standard for general purpose logic circuit design. The Parallel Interface is an extension of this circuitry to communicate with other TTL-compatible devices outside the module.

6. COMPETITIVE STANDARDS: MOS logic

7. STANDARDIZATION STATUS: Informal standards.

8. IMPLEMENTATION STATUS: Used universally as the input or output method for digital equipment.

9. KNOWN PROCESS CONTROL USES: On-off switches, relays, thumbwheel switches, analog-to-digital converters, shaft encoders, other computers, digital instrumentation, synchro-to-digital converters, counters, computer periheral devices, indicator lamps, logic devices.

10. KNOWN SOURCES OF INFORMATION: Richard Markley, US Bureau of Mines, Washington, D.C.

11. BIBLIOGRAPHY: Jules Finkel, Computer Aided Experimentation: Interfacing to Minicomputers, (John Wiley + Sons, New York).

12. COMMENTS: The nominal binary signal levels are 0 V and +3 to +5 V. The definition of the "1" and "0" levels is arbitrary and depends on the manufacturer of the equipment. The timing and clock rate is determined by the external system to which the device is communicating via the parallel interface. It should be emphasized that the parallel interface is simply an extension of the TTL logic signals within the digital device.

1. DESIGNATION: Current Loop Interface

2. TITLE: 20 MA Current Loop Interface

3. MAINTENANCE AUTHORITY: Teletype Corporation

4. SCOPE: De facto hardware and code standard. This standard defines the requirements for bit serial character transmission on a twisted pair cable. It encompasses a very simple Data Bus line and its interface electronics and also defines the conept of operator and information flow on the twisted pair and the electrical format to be employed.

5. RELATIONSHIP TO OTHER STANDARDS: RS 232-C: Similar to this, but whereas RS 232-C specifies voltage levels and control signals, simple TI specifies current levels. TI also specifies the character code (ASCII), where RS 232-C only specifies electrical characteristics.

6. COMPETITIVE STANDARDS: RS 232-C, simple TTL transmission.

7. STANDARDIZATION STATUS: Informal standard. The low transmission speeds and simple asychronous start-stop operation of the typical devices it services do not require stringent interface specifications, and almost all manufacturers produce fully compatible interfaces.

8. IMPLEMENTATION STATUS: One of the most popular interfaces for low speed interactive devices such as teletypewriters.

9. KNOWN MANUFACTURING USES: The Current Loop Interface is primarily on interface to low speed interactive devices such as teletypewriters, and CRT's. Recent products now make it possible to communicate with analog-to-digital converters and digital-to-analog converters with this interface.

10. KNOWN SOURCES OF INFORMATION: Teletype Corporation, Analog Devices, Inc., (see Bibliography), Richard Markley, US Bureau of Mines, Washington, D.C.

11. PROBABLE SOURCES OF INFORMATION: Most makers of keyboard terminals.

12. BIBLIOGRAPHY: "Product Guide," Analog Devices Inc, P.O. Box 280, Norwood, MA 02032, pp. 146-148. "Technical Manual, Model 35, Bulletin 280B, Volume 1, Teletype Corporation, Skokie, IL.

13. COMMENTS: The 20ma level signifies a binary 1, and 0 current or an open circuit signifies a binary 0. But some equipment uses 60ma instead of the 20ma. These currents have fairly high noise immunity and may be transmitted over great lengths of unshielded twisted-pair lines.

STANDARDS FOR THE SYSTEM CONTROL INTERFACE

While the functions of the system controller are fairly well defined, such is not the case with the architecture of the communications network by which the system controller coordinates and integrates the four AES functions. It should be realized that interfaces at the system level are generally more complex than at the local instrumentation level. In addition to the physical, electrical, and procedural aspects of an interface, protocol becomes an important factor at the system control level for governing the flow of data across the communications links to the functional controllers.

Mentioned previously were three communications network organizations that are applicable to the AES development: the "star", the "bus", and the "ring." As different as the architectures is the difference in their requirements for interface standards. Each will be examined to identify the appropriate interface standards which apply. Summary data sheets for these standards are included at the end of this section while Appendix B includes a comprehensive discussion on each standard.

Star Configuration

The star network configuration shown in Figure 6 is sometimes referred to as "centralized" since all communications control is focused at one common location. Message routing is done through the network controller. The network control functions relating to job scheduling, prompting, and disseminating data to the nodes are all done from a central location. They can either be accomplished by a computer dedicated to that function or by a host computer that alternates between the network-control mode and a background processing mode.

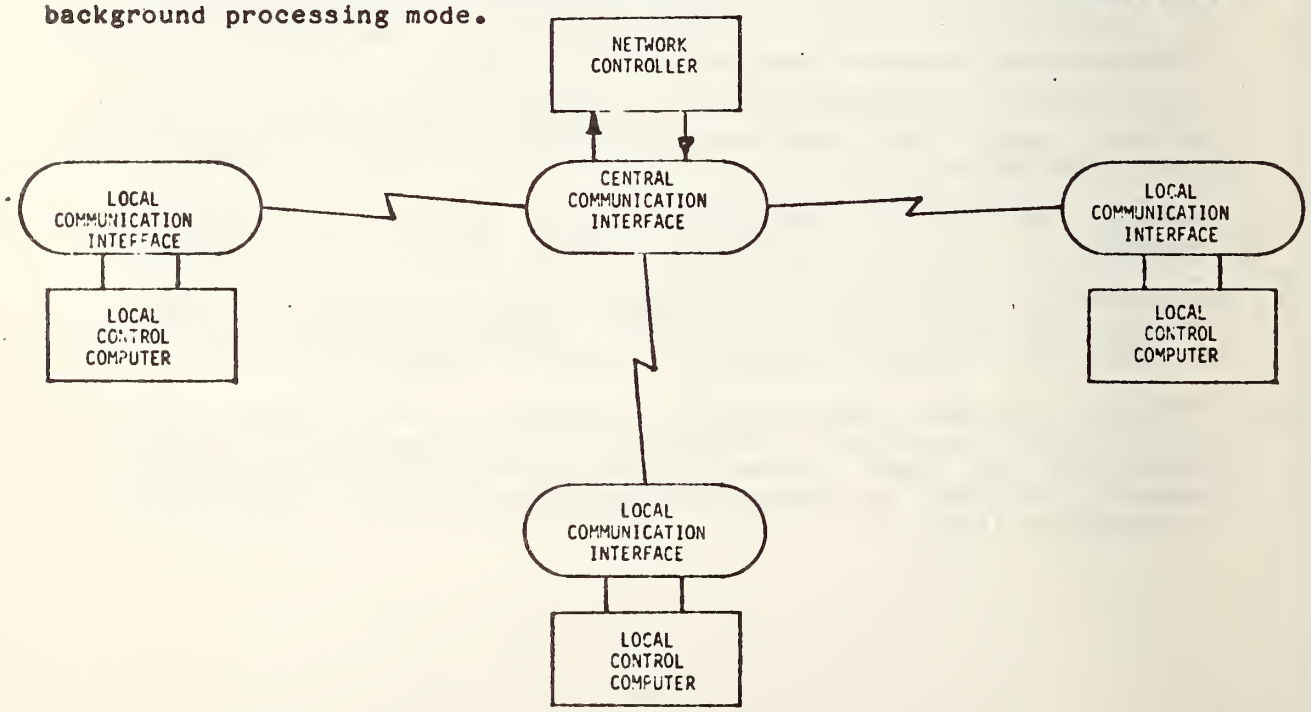


Figure 6

Because network control takes place at one location, the network control problem is greatly simplified. This type of network is directly applicable in a hierarchical process control organization since supervisory functions can be done by the central node while it manages the network. Communications with the functional controllers is concerned with task initiation, status checking, etc. Neither data rate nor volume is demanding. A bit serial, two way form of communication such as allowed by RS 232-C would suffice. If the cable length limit of 12 meters or the bit rate limit of 20 kilobits per second preclude the use of RS 232-C, serious consideration should be given to its successor, RS-449. In the unbalanced mode this will allow cable runs up to 60 meters and bit rates up to 100 kilobits. In the balanced mode RS-449 can operate to 1200 meters and 10 megabits per second.

The main disadvantage of the star network is that each communnications line applies to just one computer. Therefore, for two local control computers to communicate, their traffic must be switched through the control node. The star structure does not allow direct communications between outer nodes. As the need for dynamic interaction between outer nodes increases, more demands are made on the central network controller, and it may introduce more delays than can be tolerated in the process.

Bus Configuration

The bus structure overcomes the dynamic interaction problem by permitting simultaneous transmission of messages to all system nodes. The computer at an addressed node recognizes its address and accepts messages directed to it. Each node participates in the network control function as shown in Figure 7.

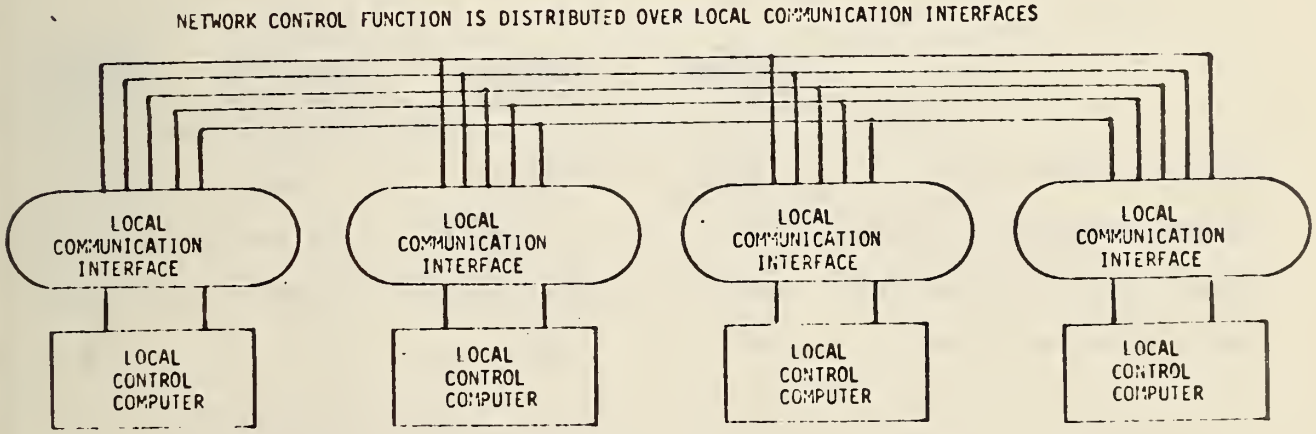


Figure 7

In general, if properly designed, distributed networks such as this offer increased reliability since a failure at one node does not necessarily affect the rest of the network. In some cases, a bus structure may facilitate testing since the testing device itself can be attached while the entire system is functioning. Similiarly, additional functional modules can easily be added to the system controller. No hardware changes are necessary. Only the software for the system controller need be modified.

For these reasons the bus structure has found wide acceptance in a variety of applications. While many of these schemes are specific to a single company or product, there are three bus structures formally documented and in the public domain which may be applicable to the AES project.

IEEE 583 - CAMAC
IEEE 488
MILSTD 1553A

All three specify completely the bus interface as to electrical, physical,procedural and higher level protocols. Table 2 compares briefly the features of these bus schemes. A more comprehensive discussion of each of these bus standards is given in the Appendices.

Table 2 - Comparison of Bus Schemes

	IEEE 488	IEEE 583 Parallel	IEEE 583 Serial	MILSTD 1553A
Maximum Length of Bus	12 m	100 m	2000 m	100
Maximum Number of Devices	15	7 crates	62 crates	32
Typical Byte Transfer Rate	1000 K hz	200-800 K hz	40-800 K hz	100
Number of Wires in Bus	24	132	2 or 4	2

The main problems with bus structures are that they are difficult to control and that they require complex communications - network interfaces at each node. Because of the generality of a bus structure, control protocol becomes complicated and priority determination becomes difficult. Contention for the bus may be resolved by giving priority to these subsystems which are physically closest to one end of the bus - this is the scheme used to resolve contention on the Digital PDP-11 "Unibus." Another method for establishing priorities is to install a bus controller which polls the subsystems at pre-programmed rates to offer them the use of the bus. The polling method eliminates all contention problems. This is the case with the three formal standards.

Ring Configuration

The third network is the loop or "ring" network illustrated by Figure 8 in which all traffic derived from the nodes is carried by a loop circuit. One of its main advantages is that it allows priority determination without a master computer. One method by which it can achieve this in a system with fixed message lengths is to employ "lazy susan" time multiplexing, in which any node can add a message to any empty circulating slot. The ring network is suitable in a process control system organization where there is complete distribution of functions and where much data must be dynamically exchanged among nodes. The nodes may have control tasks distributed to them as with the AES, or computer function tasks such as distributing the process I/O, man-machine interface I/O, stored paramters, and the computing functions.

Because each node participates in message forwarding, a failure in any node could cause complete system failure. Another disadvantage is that as messages circulate, delays occur in each node, so that this type of network may not be applicable in time critical applications.

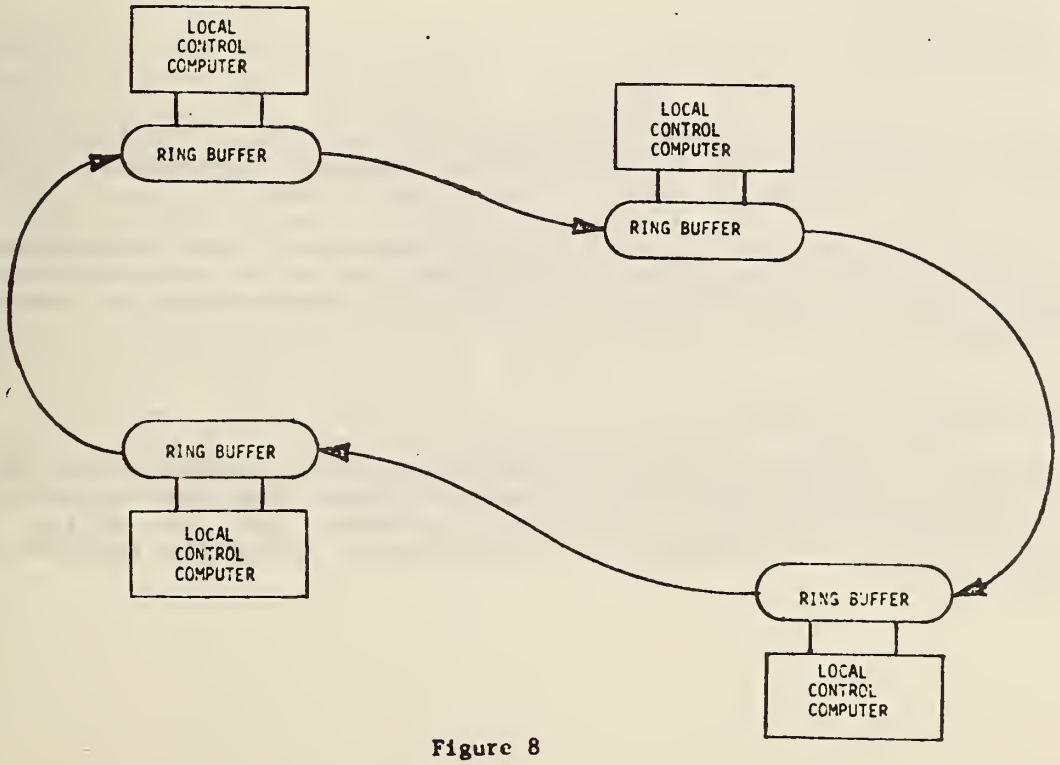


Figure 8

Data Link Control Procedures

To this point the discussion has centered on the mechanical, electrical and procedural aspects of a communications interface. This covers how the data is transmitted and how it is interpreted by the receiver. Still to be answered is the control of the communication process - the protocol that assures that the data is sent to the proper destination and that it is received without error. To do this we must look at the communications link and the control procedures that govern the process.

Anyone who has worked with automation equipment realizes the consequences of errors in the control data. Whether they be caused by data being sent to the wrong location, electrical noise, loose connections, or corroded contacts, the results are the same - lost production and often a damaged machine. Consider, then, the control of automated functions on board the coal extraction machine or possibly the control of several AES machines from a central point. In such sophisticated equipment, where malfunctions may be hazardous to human operators, there is no room for error. It is in these sensitive communications areas that link control protocol becomes essential.

Use of a link to transmit data involves not only the transmission of data but the transmission of "control" information which is used by the terminals on the link to correctly handle individual messages, to synchronize operations, and to detect and recover from errors.

Specifically, this control information should implement at least the following functional requirements:

transmission initiation
transmission control
error checking
error recovery
transmission termination

Two general types of data link control procedures may be identified: (1) the character-oriented, in which defined "control" characters delimit information fields and convey logical signalling information; and (2) the bit-oriented, in which bit strings of varying length delimit fields and convey control information. Bit-oriented procedures are recognized as inherently more efficient in terms of bandwidth, but prior to the maturation of microcomputer technology, were felt to be too computationally demanding for widespread use.

Character Oriented Protocols

The procedures of American National Standard X3.28-1976 treat the bit stream as a sequence of characters. This standard utilizes the ten communications control characters of the ASCII (ANSI X3.4) character set to define link control and specify procedures for establishing, using and terminating a link connection.

A problem with X3.28 is that the standard, rather than giving a single solution to the problem of link control, is essentially a list of approved alternative solutions. Ten subcategories of establishment/termination procedures are specified and fourteen subcategories of message transfer procedures. Thus, there are 140 possible systems which are standardized by X3.28. However, only about 80 of these can actually be realized, and most of these systems are incompatible with each other.

Bit Oriented Protocols

Bit oriented procedures have been advanced both because of their inherently higher efficiency (in terms of line utilization) and as a way to "start fresh" from the maze of different configurations in X3.28. Until recently, these procedures were limited due to the computational complexity of framing, "bit-stuffing" and error detection computing. But the new microprocessor technology has opened the way for the widespread application of this type of procedure.

The American National Standards Institute is currently developing a proposed standard called Advanced Data Communication Control Procedures (ADCCP) which approaches the same problem as X3.28-1976. Though a number of years in development by ANSI the new bit-oriented data link control procedure is finally near completion. The unit of transmission in ADCCP is a frame, and all transmissions on the link utilize this format. ADCCP is basically divided into three parts. The first part includes the frame format specifications and a description of the 16 bit algorithm used for error detection in the frame check sequence. The second part describes the modes of operation and repertoire of commands and responses. The final part of ADCCP deals with the six different classes of procedure that are allowed under the standard. A user would choose the one best suited to his mode of operation.

ADCCP entails three different methods of error detection. The 16-bit Cyclic Redundancy Check (CRC) polynomial metioned before is used for detecting errors in transmission. In addition, a response timer is specified for the primary station, to detect no response from the secondary station. The sequential numbering of frames also helps detect lost or duplicated frames.

Placing this in terms of what ADCCP means to a user is quite simple. On a serial communications link a user could specify RS 449 for the mechanical, electrical, and procedural aspects of his communication and ADCCP for the protocol. With this configuration handling the data communications between the AES systems controller and each of the functional controllers, a user would have the total assurance of good data communications required for remote operation. It has been demonstrated with such a system that one can momentarily unplug the communication link without introducing errors into the industrial process. ADCCP handles all of the error detection and retransmission needed to assure error-free end to end communication.

Summary Data Sheets

The following pages list summary data on the various standards mentioned in this section on the System Control Interface. Included here are the following:

IEEE Standard 488
IEEE Standard 583
MIL Standard 1553 A
ANSI X3.28
ANSI ADCCP

1. DESIGNATION: IEEE Standard 488-1975

2. TITLE: IEEE Standard Digital Interface for Programmable Instrumentation

3. MAINTENANCE AUTHORITY: IEEE Instrumentation and Measurement Group

4. SCOPE: Hardware Standard. This standard applies to interface systems used to interconnect both programmable and non-programmable (digital) electronic measuring appartus with other apparatus and accessories necessary to asemble instrumentation sysytems. It is a parallel-by-bit, serial-by-byte standard.

5. RELATIONSHIP TO OTHER STANDARDS: The character coding is based upon ISO 646-1973, similar to ASCII, FIPS PUB 1, ANSI X3.4-1968.

6. COMPETITIVE STANDARDS: EIA RS-408, IEEE Standard 583-1975 (CAMAC)

7. STANDARDIZATION STATUS: Approved by the IEEE Standards Board on December 19, 1974. Development of this standard was coordinated with IEC/TC66/WG3. It may become an IEC standard.

8. IMPLEMENTATION STATUS: Implemented in electronic instruments, such as those made by the Hewlett-Packard Co.

9. KNOWN MANUFACTURING USES:

10. KNOWN SOURCES OF INFORMATION: Mr. Robert A. Soderman, General Radio Co., (617)396-4400 x608; Mr. Donald C. Loughry, Hewlett-Packard Co., (408)735-1550; Mr. Robert G. Fulks, Omnicomp, 71 N. 12th Place, Phoenix, (6020997-5456.

11. PROBABLE SOURCES OF INFORMATION: Mr. Barry A. Bell, NBS, (301) 921-2727.

12. BIBLIOGRAPHY: IEEE Standard 488-1975

13. COMMENTS: Up to 15 devices may be interconnected on one "party-line" configuration. Cable length is up to 20 meters. Maximum data rate on an any signal line is one megabit per second. This standard is optimized for devices in close proximity (up to 20 meters).

1. DESIGNATION: IEEE Standard 583-1975

2. TITLE: IEEE Standard Modular Instrumentation and Digital Interface Systems (CAMAC)

3. MAINTENANCE AUTHORITY: IEEE Nuclear Instruments and Detectors Committeee

4. SCOPE: Hardware Standard. "This standard is intended to serve as a basis for a range of modular instrumentation capable of interfacing transducers and other devices to digital controllers for data and control. The standard fully specifies a data bus by means of which instruments and other functional modules can communicate with each other, with peripherals, with computers, and with other external controllers. Data may be transferred either bit-serial or byte-serial."

5. RELATIONSHIP TO OTHER STANDARDS: Identical in many respects to IEC 482 and 516.

6. COMPETITIVE STANDARDS: EIA RS-408, IEEE Standard 488, EIA RS 232-C

7. STANDARDIZATION STATUS: Approved by the IEEE Standards Board on February 27, 1975.

8. IMPLEMENTATION STATUS: Increasingly implemented in laboratory digital instrumentation equipment, especially that related to nuclear physics and testing.

9. KNOWN MANUFACTURING USES: Aluminum Furnace Control (ALCOA), Steel Process Control (Inland Steel Co.), Diesel Locomotive Testing (GM), Large Power Semiconductor Testing (GE), Telescope Control and Data Gathering (Kitt Peak)

10. KNOWN SOURCES OF INFORMATION: Mr. Dale W. Zobrist, Eldec Corporation, (206)743-1313; Mr. Louis Costrell, NBS, (301)921-2518; Mr. Lowell A. Klaisner, Kinetic Systems Corporation, (815)838-0005.

11. PROBABLE SOURCES OF INFORMATION: IEEE, ERDA, Stanford Linear Accelerator Center, Lawrence Radiation Lab, Berkeley, CA.

12. BIBLIOGRAPHY: IEEE Standard 583-1975; "CAMAC, A Modular Standard," IEEE Spectrum, April 1976, pp. 50-55.

13. COMMENTS: This standard was developed by the ESONE Committee of European Laboratories and the NIM Committee of ERDA. Data may be transferred byte-serial for high speeds and bit-serial for long distance.

1. DESIGNATION: MIL-STD-1553A

2. TITLE: Aircraft Internal Time Division Command/Response Multiplex Data Bus

3. MAINTENANCE AUTHORITY: Standards groups, ENESS, Aeronautical Systems Division, Wright-Patterson Air Force Base, Ohio, 45433.

4. SCOPE: Total bus standard. This standard defines requirements for digital, command/response, time division multiplexing (Data Bus) techniques on aircraft. It encompasses the Data Bus line and its interface electronics and also defines the concept of operation and information flow on the multiplex data bus and the electrical and functional formats to be employed.

5. RELATIONSHIP TO OTHER STANDARDS: MIL-STD-461 Signal quality requirements for equipment incorporated on this bus.

6. COMPETITIVE STANDARDS:

7. STANDARDIZATION STATUS: MIL-STD-1553 (USAF) 30 August 1973, MIL-STD-1553A, 30 April 1975.

8. IMPLEMENTATION STATUS: Is being installed on various military aircraft including the F-16, F-18 and Army advanced armed helicopter (AAH).

9. KNOWN MANUFACTURING USES: MIL-STD-1553A is primarily a high performance bus specification for aircraft.

10. KNOWN SOURCES OF INFORMATION: Mr. Charles Gifford, ENESS, Wright Patterson Air Force Base, Dayton, Ohio, (513)255-4130.

11. PROBABLE SOURCES OF INFORMAION: Harris Semiconductor Co., SCI Systems Corporation, Huntsville, Alabama.

12. BIBLIOGRAPHY: MIL-STD-1553A, 30 April 1975.

13. COMMENTS: The multiplex bus standard is relatively stable and is unusual because of the long length (up to 100 meters), at low permissible error rate (10-12) in conjunction with a remote terminal, and the fact it only requires 2 wires. The bus is expensive - all units built to data have been custom built. USAF is sponsoring LSI development for modular interfaces but it will be at leat 1 1/2 years before a product is delivered. Avionics vendors prefer to install the entire avionics package.

1. DESIGNATION: ANSI X3.28-1976 Communication Protocol (Link Level) Standards - Character Oriented

2. TITLE: Procedures for the Use of the Communication Conrol Characters of ASCII in Specified Data Communication Links

3. MAINTENANCE AUTHORITY: ANSI X3S3, Task Group 3

4. SCOPE: Protocols for Link Level Data Communication

5. RELATIONSHIP TO OTHER STANDARDS:
ANSI X3.4 (ASCII Character Set, Control Characters Used to Format Transmission)
ISO R1745-1971 (Dialect)
ECMA-16, 1973 (Dialect)
ISO R2111-1972 (Extension to Base Mode for Code-Independent Information Transfer)
ISO R2629-1973 (Extension to Basic Mode for Conversational Information Transfer)
ECMA-24, 1969 (Extension to Basic Mode for Code-Independent Information Transfer)
ECMA-26, 1971 (Extension to Basic Mode for Recovery Procedures)
ECMA-27, 1971 (Extension to Basic Mode for Abort and Interrupt Procedures)
ECMA-28, 1971 (Extension to Basic Mode for Multiple Station Selection)
ECMA29, 1971 (Extension to Basic Mode for Conversational Information Transfer)
ECMA-37, 1972 (Extension to Basic Mode for Supplementary Transmission Functions)

6. COMPETITIVE STANDARDS: IBM's Binary Synchronous Communications, BISYNC/IBM Order No. GA27-3004- 2/10/70 (more extensive than X3.28, and utilizing EBCDIC Character Set).

7. STANDARDIZATION STATUS: Revised Standard Issued in 1976.

8. IMPLEMENTATION STATUS: No known implementations adhering strictly to the standard classes of procedures. Each computer manufacturer has implemented a different part of X3.28. The standard specifies approximately 140 different system configurations that can be implemented conforming to the standard.

9. KNOWN MANUFACTURING USES:

10. KNOWN SOURCES OF INFORMATION: Mr. George E. Clark, NBS, (301) 921-3723.

11. PROBABLE SOURCES OF INFORMATION:

12. BIBLIOGRAPHY: ANSI X3.28-1971, "Procedures for the Use of the Communication Control Characters of American National Standard Code for Information Interchange in Specified Data Communication Links", American National Standars Institute, Inc., New York, NY, 10018.

13. COMMENTS: Not a FIPS standard because does not provide for compatibility and data interchange among different systems.

1. DESIGNATION: ANSI X3S34/589 (Draft 5) Communication Protocol (Link Level) Standards - Bit Oriented

2. TITLE: Proposed ANS for Advanced Data Communication Control Procedures (ADCCP) (Draft 5, 4/9/76)

3. MAINTENANCE AUTHORITY: ANSI X353, Task Group 4

4. SCOPE: Hardware/Software. The (proposed) standard establishes procedures to be used on synchronous communications links.

5. RELATIONSHIP TO OTHER STANDARDS: IBM Synchronous Data Link Control (SDLC) is a subset of ADCCP. IBM Document GA27-3093-1

6. COMPETITIVE STANDARDS: ANSI X3.28 (Character oriented), IBM BISYNC (Character oriented), DEC DDCMP

7. STANDARDIZATION STATUS: Draft 5 being circulated for letter ballot.

8. IMPLEMENTATION STATUS: No known implementation operational. IBM's SDLC may be functional a this time. A number of microprocessor chips are being developed to be used as ADCCP link controllers; one known effort is Motorola.

9. KNOWN MANUFACTURING USES:

10. KNOWN SOURCES OF INFORMATION: ANSI Committee X3, Tech. Committee X3S3, Task Group 4; Mr. George E. Clark, NBS, (301) 921-3723.

11. PROBABLE SOURCES OF INFORMATION: IBM, Honeywell

12. BIBLIOGRAPHY: ANSI X3S34/589 (Fifth Draft) 4/9/76, Advanced Data Communication Control Procedures, American National Standards Institute.

13. Donnan, R. A., and J. Ray Kersey, "Synchronous Data Link Control: A Perspective", IBM Systems Journal. 2, 197.

14. Sanders, R. W., and V.G. Cerf, "Compatibility or Chaos in Communications", Datamation, 3/76, pp. 50-55.

15. COMMENTS: IBM is known to be basing most of its networking efforts on the use of SDLC as a link-level protocol.

CONCLUSION

The U.S. Bureau of Mines automatic coal extraction system (AES) identifies two levels in the control system for which standards must be established: the local instrumentation level and the system control level. The local instrumentation interfaces are those between the local computer based functional controllers and their respective sensors and actuators. The system control interfaces include those between the system control computer and the functional modules and those between the functional modules themselves. The use of formal standards to characterize these various interfaces simplifies the definition and results in a system configuration which is easily maintained and offers the flexibility for future incremental modification without a total system redesign. This report identifies, analyzes and explains those interface standards which may be applicable to the design of an automated computer based control system for the AES.

Local Instrumentation Interface

The simplest interface to instrumentation that generates analog signals between +/- 10 volts and is less than 12 meters away (the order of AES) is straight analog. Noise problems can be minimized by proper shielding and the use of a balanced or differential signal transmission line. An analog multiplexer operating in a differential mode antecedent to the analog to digital converter would permit multiplexing many analog signals to the computer, allowing multiple use of the analog to digital converter which would reduce costs. A digital voltmeter or oscilloscope can be used for testing and a standard voltage source can be used to test the computer's ability to read the analog data. Calibration of the sensor, if the actual voltage levels are important, will be a recurring problem.

Several sensors are available with self test and calibration features which can be initiated electronically. These are called "smart" sensors and their use should be encouraged wherever possible. In the long term, all of the sensors and actuators should have this feature. Their use, however, poses a new problem; the need for two way computer-sensor communication. With the use of "smart" sensors and actuators, NBS recommends a two wire digital serial communication link from the sensor to the computer that will include digitizing and data conversion electronics. The EIA RS 232-C or RS-449 interface standards are recommended for this application. The same microcomputer in the sensor package can provide the ADCCP protocol needed for error free communication with the functional controller.

When on-off signals to devices such as relays and indicator lamps must be transmitted, onboard the AES we recommend that all tranmissions be done at TTL logic levels (0 to 5 volts). Actuators should be designed so that all high voltages needed for operation are locally supplied, not transmitted from the computer site. This is primarily a safety precaution, but it also eliminates noise transfer between cables resulting from alternating currents and transient spikes. Line drivers are problably not necessary as long as the wiring distance is less than 12 meters. Severe noise may require redundancy checks or optical couplers to isolate system, components.

APPENDICES

System Control Interface

The system control interface is more difficult to specify because it is largely a function of speed and accuracy of data transfer required by the modules and system controller. As before, simplicity, maintainability, flexibility, and cost are also important. For low speed point to point communications a simple RS 232-C or RS-449 interface may be sufficient. For high speed multipoint communications a high performance bus might be required.

In the first case with RS 232-C the ASCII code is recommended. For all digital serial communication links use of a link control protocol such as ADCCP. is essential to assure that data is sent to the proper destination and is received without error. Either 2-wire half duplex or 4-wire full duplex mode of operations could be used depending on data volumes needed. The RS 232-C would be most applicable to a star network configuration where data is being transferred between the system controller and the functional modules at up to 1000 characters per second and there is little need for module-to-module communications. RS-449 is preferable for higher speeds but some difficulty may be experienced in the near future in obtaining LSI chips to facilitate implementation of this new standard. Several multiplexers are available which would provide multiple use of the computer communication port.

If more data is transferred in the system or if a large degree of functional module-to-functional module data transfer is required, a Bus network may be necessary. In this case, we recommend the IEEE 488, because it does not put mechanical constraints on the hardware as does IEEE 583 (CAMAC). The MILSTD-1553A standard is good but very expensive. The IEEE 488 bus will permit data transmission at 1 million characters per second within the system, and its specification includes protocol. One disadvantage is that testing equipment may have to be provided. However, if a Bus to RS 232 C interface is available (as is the case with IEEE 488) (2) it will be possible to test the system to a certain degree using a CRT. We recommend that this interface be included with any Bus to facilitate testing.

Summary

It is realized that the Bureau of Mines will be faced with many decisions regarding interface specifications in the AES control system development. This report is not intended to be a recommendation for a specific design but rather to serve as a technical guide and summary of existing and forthcoming interface standards that may be applicable to the project. The use of formal standards to specify the interfaces between modular elements of the AES control system will not restrict the design freedom of vendors but will result in a system that is more understandable, more maintainable, and more flexible for future incremental expansion and enhancement.

STATEMENT OF WORK

Objective

The Bureau of Mines is engaged in the development of a modular control system for face equipment which has automated subsystems to control such underground mining tasks as the cutting cycle, guidance, roof support, and roof bolting. The National Bureau of Standards has discussed with the Bureau the interface problems inherent in this modular control system. These interfaces range from the sensor-to-controller interface, which may be analog or digital communication, to the onboard controller-to-remote supervisory computer which is normally digital communication. This project will recommend the most appropriate interface standards to apply in cases as this, which, among other benefits, will improve project management and the final assembly of vendor-developed subsystems.

1. To identify those current analog and digital standards relevant to sensor-based equipment.

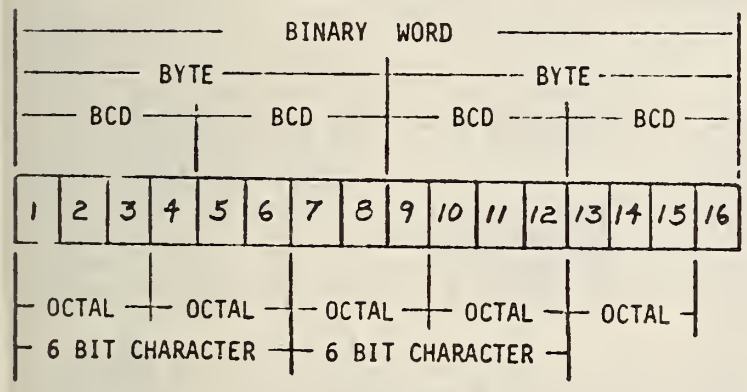
2. To analyze those standards and determine their merit to the Bureau of Mines Project.

3. To recommend on the basis of National Bureau of Standards experience and expertise, with the findings in 1 and 2 above, the most appropriate standards for the sensor-to-controller interface, possible subsystems controller-to-system control interface, and system controller-to-supervisory control system interface.

Digital I/O (TTL)

For interfacing instrumentation to a computer the lowest level standards include the electrical standard which for most computers is a logic level specification. The integrated circuits most commonly used in logic design are based on transistor/transistor logic (TTL), "which may be regarded as the industry standard for general-purpose logic circuit design." Many instruments are available such as analog to digital converters, thumbwheel switches, and shaft encoders with output interfaces provided in "TTL-compatible" form. Similarly, devices such as digital to analog converters, analog or digital multiplexers, and indicator lamps can be actuated by TTL-compatible signals which may be supplied by a digital parallel output computer peripheral.

The data transfer may be in serial or parallel form. Most digital data sources provide parallel outputs in preference to serial outputs. Although serial data makes wiring simpler, decoding of the data must be done at the receiving end of the serial line making the circuit more complex. There are several ways of packing the data in a parallel output. Typical analog to digital converters and digital panel meters output data in binary or binary coded decimal (BCD) format. The binary word can be arranged in groups of 3 bits to form octal digits that simplify representation of the word. Figure 9 shows these various methods and the resulting codes.



Decimal	Binary	Octal	BCD
0	000	0	0000
1	001	1	0001
2	010	2	0010
3	011	3	0011
4	100	4	0100
5	101	5	0101
6	110	6	0110
7	111	7	0111
8	1 000	1 0	1000
9	1 001	1 1	1001

Figure 9

Typically, the computer peripheral which interfaces to the digital parallel devices will have as many lines available for input or output as there are bits in the computer's word length. Thus an 8-bit microcomputer would have circuits which exchange 8 bits of data at a time and a 16 bit minicomputer would have circuits which exchange 16 bits of data at a time. Of course, if a device had more information than could be transferred at one time through one circuit, more circuits could be added and the computer could handle them sequentially. This is what is usually done by an 8 bit microcomputer which requires data from a 12 bit analog to digital converter.

Technical Specifications

Integrated circuits of the TTL type all have bipolar logic. Because of the universal application of bipolar logic, voltage levels encountered in interface design are relatively standard at 0 V and +3 to +5 V. Either voltage may be designated as the "one" or "true" state to assure that an open circuit to a sensor or actuator is not mistaken for a true condition.

The output drive capability of a TTL circuit is designated as its "fan-out." This is a number which represents the number of unit loads that the circuit can drive. It is important to consider when the output of, say, the computer, will be used to drive several digital circuits. Ordinary TTL circuits have fan-outs of between 5 and 10 with the actual fan-out usually defined by the manufacturer of the equipment. Of equal importance is the "fan-in" of the circuit to be driven. Thus, a logic element with a fan-out of 10 can drive normalized input logic elements with a total fan-in of 10 or less. Reliable operation is assured if the manufacturer's worst case analysis of the circuits being considered is followed.

Typical Application

There are many applications involving the direct interface of digital instrumentation to digital computers which illustrate the utility of the TTL specifications in a control environment. Figure 10 depicts a method of computer control for a laboratory manipulator developed at NBS. The computer is a DEC PDP11/45 with a DR-11C parallel digital interface permitting 16 lines of data input and 16 lines of data output. The DR-11C is connected to the laboratory equipment 35 meters away by forty parallel wires powered by 7406 line drivers. The laboratory interface hardware consists of two parts: an input section and an output section.

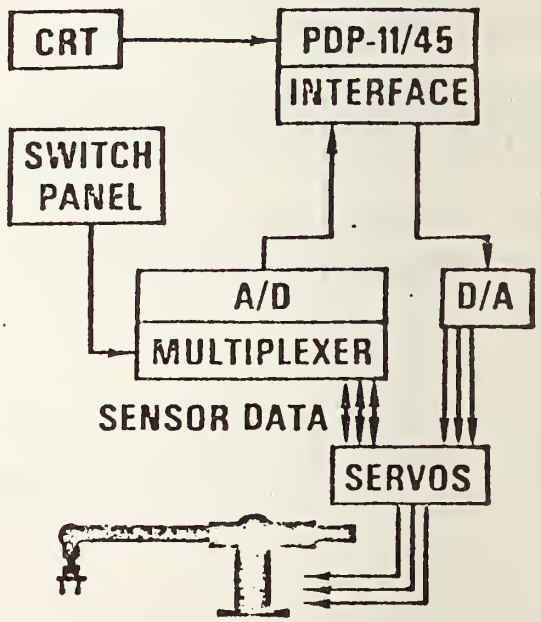


Figure 10

Input Section - A sixty-four channel analog multiplexer followed by a 14 bit analog to digital converter forms the heart of the input section. This accepts analog signals in the range of -10 volts to +10 volts. Negative voltages are converted to 2's complement form.

Output from the A/D converter is carried to the computer on the 16 data input lines. Since the A/D converter has only a 14 bit output, the most significant (sign) bit is connected to the three most significant computer input lines. This causes the computer to read the correct values for both positive and negative (2's complement) numbers.

Data transfer between the A/D converter and the computer is signaled by a pulse on the data transmitted line. This pulse, initiated by the computer, indicates that the data lines have been sampled. The data transmitted pulse is used both to step the analog multiplexer to the next input and to initiate the analog to digital conversion cycle on the new input voltage. The input software is timed to sample the input data at a rate slower than the conversion rate of the A/D system. Thus, a "conversion completed" signal is not required by the computer, and only one control line is needed to advance the converter to the next channel.

The multiplexer is operated in a sequential mode. It is reset to channel zero by a reset pulse derived from the output section. Each data transmitted pulse steps the multiplexer to the next sequential channel. The input section is thus completely under computer control.

Output Section - A sixteen channel digital demultiplexer routes output signals from the DR11-C to sixteen holding registers. These provide either digital output directly, or are connected to digital to analog converters so as to provide analog voltages. Data transfer between the DR11-C and the output section is initiated by a pulse on the data present line. The data present pulse occurs simultaneously with the appearance of data on the DR11-C output lines. This pulse is delayed in the laboratory interface hardware for two microseconds before actuating the digital demultiplexer so as to allow time for the data lines to settle. The delayed data present pulse gates the output data into the selected holding register and then steps the address counter to the next address.

The most significant (sign) bit of the output is decoded as a reset signal and is used to set the demultiplexer address counter to Channel 1 as well as to reset the analog multiplexer address in the input section.

Using the sign bit for control means that only 15 bits of output are available for data. The numerical range is thus restricted to 0 to 32,767. The digital to analog converters are adjusted such that numerical 0 corresponds to +10 volts, 16,384 to zero volts, and 32,767 to -10 volts.

References

Finkel, Jules, Computer Aided Experimentation: Interfacing to Minicomputers (John Wiley, New York) 1975

NBSIR 75-973 "Guide to Improving the Performance of a Manipulator System for Nuclear Fuel Handling Through Computer Controls" John Evans, Jr., et al., November 1975.

20 MA CURRENT LOOP INTERFACE

One of the most popular, though informal, standards for low speed telecommunications is the 20 milliamp current loop interface. Developed originally by the Teletype Corporation and now quite widely used, the data transmission scheme has never achieved formal standardization. It is generally used for simple low speed applications.

The standard is usually applied to teletypewriters and other keyboard terminals such as CRT's. The transmission rates are usually low ranging from 10 characters/sec to 120 characters/sec since these terminals are used for data transactions at the man-machine interface.

Because the standard is based on electrical current levels, it is highly immune to noise and is ideal for communications in high electrical noise environments such as shop floors and over long distances (30 to 300 meters at 600 bps) where noise pickup might introduce errors in transmission. A common application is the use of a 20 MA current loop where the terminal is a keyboard teletypewriter being used as a console to a computer.

Recently commercial modules have been introduced which include all of the circuitry necessary to communicate between a current loop serial device and a digital parallel input or digital parallel output device. This has expanded the use of this standard to where it can be applied to communication systems involving analog to digital converters, analog multiplexers, and digital to analog converters. These devices can now be used in areas where high noise often creates problems in data transmission. They can transmit at up to 19.2 kilobits per second.

Technical Description

The standard specifies a 20 MA current level in the circuit, which by simple on-off operation is used to transmit the proper code (usually ASCII characters). Figure 11 gives the code pattern showing the nominal current levels. There are times that 60 MA current levels have been used, but these are not common.

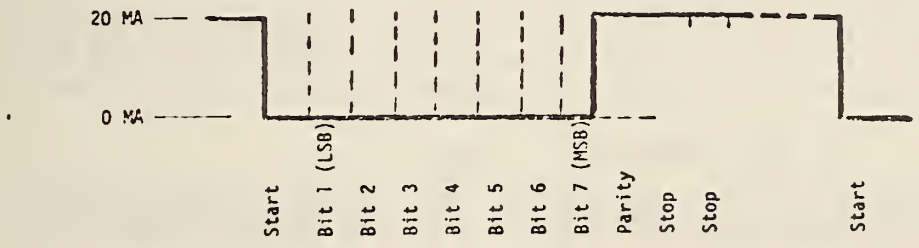


Figure 11

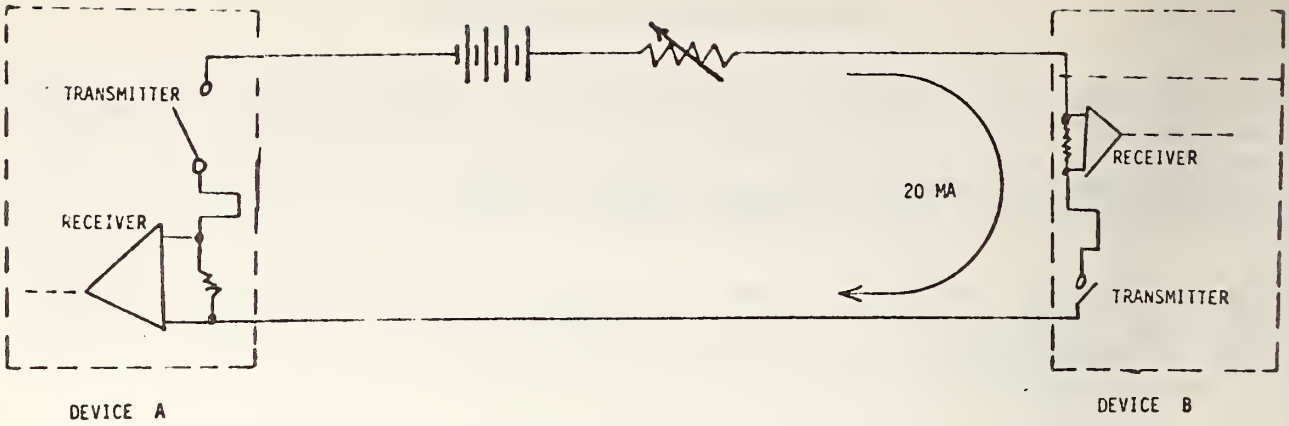


Figure 12

Each serial character consists of one start bit, seven ASCII-coded data bits, a parity bit and two stop bits. Under quiescent conditions all loop circuits are closed and 20 MA flows. A start bit, followed by the data bits is transmitted by operating one of the transmitter switches. The receiving device detects the presence or absence of current as shown in Figure 12.

Typical Application

Figure 13 illustrates an application where a teleprinter is used to interrogate a remote digital thumbwheel switch. The current loop regulator can be a simple 6 volt power supply with a variable resistor to establish a loop current of 20 MA. The two digit thumbwheel switch has 10 numbers on each thumbwheel, 0 through 9 and has a BCD complement output which interfaces directly to a transmitter card that converts the parallel inputs into a serial ASCII coded current loop bit stream. The transmitter can interface with up to 32 digital parallel inputs. In this application the two digit switch requires only eight. The transmitter card is generally run as a passive device, that is, it does not supply any current to the current loop, it acts only as a switch to interrupt the current flow as required to generate the ASCII characters.

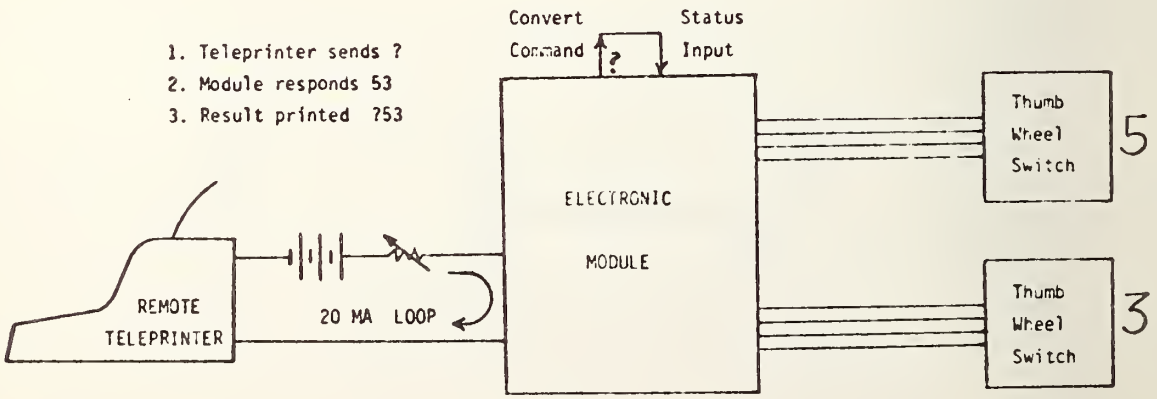


Figure 13

EIA RS 232-C

The standard interface between data terminal equipment (DTE) and data communications equipment (DCE) is Electronic Industries Association RS 232-C. The standard describes a widely used form of serial, binary data interchange. While detail is provided in reference RS 232-C, a summary of technological constraints and of interface functions is provided in this Appendix. The interface standard defines electrical signal characteristics, mechanical interface characteristics, functional descriptions of interface circuits and standard interfaces for selected communication systems configurations. The standard also contains explanations and recommendations as well as a glossary of terms. It should be noted that data must be serialized by the data terminal equipment, so that the data communications equipment may be independent of the character length and codes used by the data terminal equipment. No restrictions on bit sequence arrangements provided by the DTE must be made by the DCE.

This discussion of RS 232-C borrows liberally from previous publications at the National Bureau of Standards. (see NBS Technical Note 843)

Technical Description

The electrical interface is characterized by positive and negative voltage swings at the interface: a negative signal signifying the marking condition and a positive signal signifying the space condition. Broad voltage limits are specified for both positive and negative polarities (3 volts to 25 volts). The region between negative 3 and positive 3 volts is defined as the transition region, in which signals are not defined. Further details as to equivalent circuit configuration, circuit parameter tolerances and other detail are given in document RS 232-C.

The mechanical interface is located at a pluggable connector signal interface point. The female connector is associated with the DTE, the male counterpart with the DCE. An extension cable is provided with the DTE, and is optional with the DCE. The connector provides 25 circuits, and pin number assignment for circuits are part of the standard. Although the standard specifies that pin assignments listed in the standard shall be used, it also specifies that "pin assignments for circuits not specifically defined ... are to be made by mutual agreement. Preference should be given to the use of unassigned pins, but in the event that additioal pins are required, extreme caution should be taken in their selection."

The functional description of the interface provides for 25 circuits. Four are unassigned for use as spares. Of the 21 remaining, there are four general categories: Ground or common return, Data circuits, Control circuits, and Timing circuits. Functions assigned to the various circuits are described below.

Two distinct ground circuits are provided. PROTECTIVE GROUND is electrically bonded to the equipment frame. It may be further connected to

external grounds as required by applicable regulations. SIGNAL GROUND establishes the common ground reference potential for all interchange circuits except for the PROTECTIVE GROUND circuit.

There are two circuits which carry data.

The TRANSMITTED DATA circuit carries data from the local DTE to the local DCE and from there to the distant communications and processing equipment. When no data are transmitted, this circuit is held in the marking or OFF condition. Data cannot be transmitted unless all of the following circuits are in the ON conditions (when implemented): REQUEST TO SEND, CLEAR TO SEND, DATA SET READY, DATA TERMINAL READY.

The RECEIVED DATA circuit carries data from the receiving DCE in response to the remote DCE and DTE. This circuit is held in the OFF condition when the circuit RECEIVED LINE SIGNAL DETECTOR is in the OFF condition.

Eight control circuits are provided in RS 232-C.

The request to send circuit is used to condition the local DCE for data transmission. On a two way alternate channel this means control of the direction of data transmission of the local DCE. The ON condition maintains the DCE in the transmit mode, and in the case of two way alternate mode inhibits the receive mode. The OFF condition maintains the DCE in the nontransmit mode, and in the case of the two way alternate mode enables the receive mode. The OFF-to-ON transition puts the DCE into the transmit mode, and generates the CLEAR TO SEND SIGNAL. The ON-to-OFF transition puts the DCE into the non-transmit or receive mode.

Signals on the CLEAR TO SEND circuit are generated by the DCE and indicate to the DTE that the DCE is ready to transmit data. The ON condition, together with the ON conditions on all of the circuits: REQUEST TO SEND, DATA SET READY, and DATA TERMINAL READY, (when implemented) indicate to the DTE that signals can be transmitted on the TRANSMITTED DATA circuit. The OFF condition indicates to the DTE that it should not transmit data. The ON condition on the CLEAR TO SEND circuit is a response to the simultaneous ON conditions on circuits DATA SET READY, and REQUEST TO SEND.

Signals on the DATA SET READY circuit indicate the status of the local DCE. The ON condition indicates that the local DCE is connected to a communications channel (off-hook in switched service), and that the local DCE is not in test, alternate voice or dial mode, and that the local DCE has completed any timing functions required by the switching system. It also indicates that the local DCE has completed call establishment, and the transmission of a discrete answer tone, the duration of which is controlled only by the local data set, if these functions are implemented.

Signals on the DATA TERMINAL READY circuit go to the DCE and control switching of the DCE to the communications channel. The ON condition prepares the DCE to be connected to the communications channel and maintains

the connection established by external means, i.e. manual call origination, manual answering, or automatic call origination. The OFF condition causes the DCE to be removed from the communications channel, following completion of any in-process transmission.

The RING INDICATOR circuit ON condition received from the DCE indicates to the DTE that a ringing signal is being received on the communications channel, from the distant DCE. ON and OFF conditions correspond to the ring and no-ring signals.

The RECEIVED LINE SIGNAL DETECTOR circuit ON condition indicates that the DCE is receiving a signal suitable for demodulation. Criteria for suitability are established by the DCE manufacturer.

The standard includes a SIGNAL QUALITY DETECTOR circuit. An ON condition received from DCE indicates to the DTE that there is no reason to believe that an error has occurred. The OFF condition indicates that there is a high probability of error. This signal may be used to call for automatic retransmission of a previously transmitted signal.

Signals on the DATA SIGNAL RATE SELECTOR circuit originate at the DTE or DCE to select one of two signalling rates available in a dual rate synchronous DCE, or one of two ranges available in a dual range asychronous DCE. The ON condition selects the higher rate or range. One circuit is available for this function. The signal source may be either in the DTE or the DCE.

Three circuits provide for timing information flow between DTE and DCE.

Two of them are called TRANSMITTER SIGNAL ELEMENT TIMING. They provide timing signals, originating either from the DCE or the DTE, indicating signal element center, (DTE source) or signal element transitions (DCE source) on the TRANSMITTED DATA circuit. Only one of the circuits is employed in any particular implementation.

The other timing circuit is called the RECEIVER SIGNAL ELEMENT TIMING (DCE source). Signals on this circuit provide received signal element timing information from the DCE to the DTE. The On to OFF transition on this circuit nominally indicates the center of each signal element on the circuit RECEIVED DATA.

TYPICAL APPLICATION

One of the factors contributing to the widespread use of RS 232-C is the ease of hardware implementation. This has been made possible through LSI chips that are readily available and quite inexpensive. The basic functions for transmission are to accept data in parallel format often from a bus, convert it into a serial bit stream, add any necessary parity, start or stop bits, change the logic levels to those required by RS 232-C, and generate the control signals for the modem or receiving terminal. A similar but inverse sequence is used to receive signals. These functions can be performed by three LSI chips shown in Figure 14. The first is a Universal Synchronous/Asynchronous Receiver/ Transmitter (USART) while the second is a Logic Level Converter and the last is a Transmission Rate Generator.

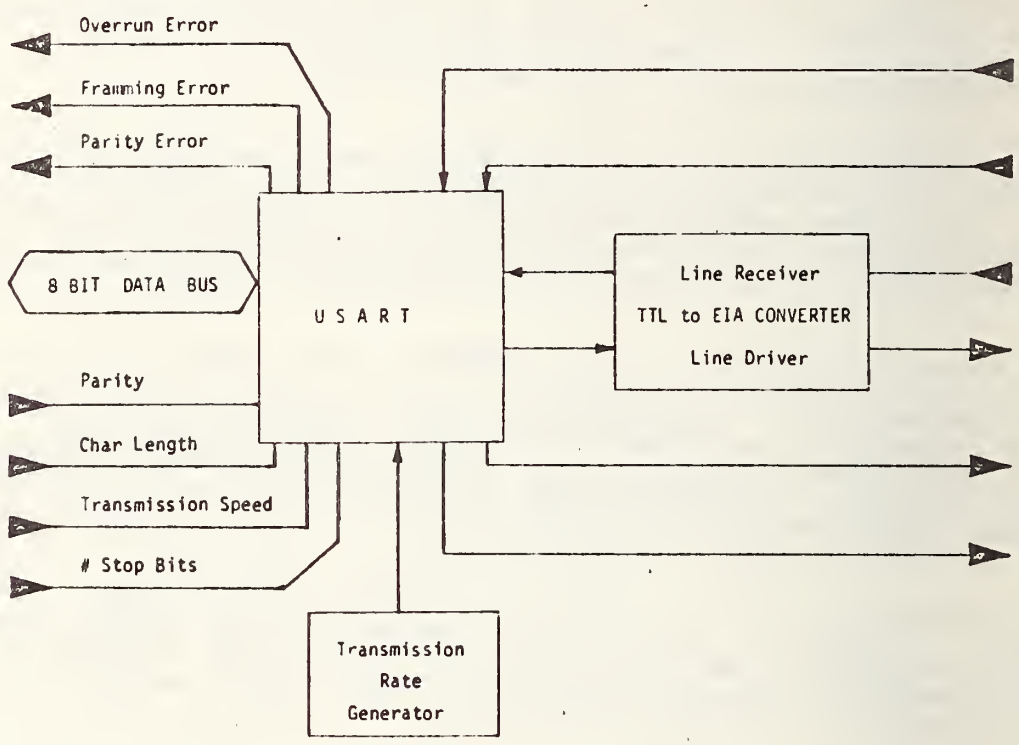


Figure 14

Although the standard specifies a maximum line length of 12 meters, the IC line drivers commonly available allow better performance. Some commercial data terminal equipment at NBS operates reliably up to 1000 meters at 2400 bits per second over four wire unshielded cable. This feature has allowed the increasing use of remote terminals without modems. An example of this simplified use of RS 232-C is given in Figure 15 detailing configuration used by NBS its Experimental Computer Facility to support a number of CRT and teleprinter terminals. Four wire unshielded cable is used. RS 232-C circuits in operation are:

TRANSMITTED DATA	Pin 2
RECEIVED DATA	Pin 3
SIGNAL GROUND	Pin 7
CLEAR TO SEND	Pin 5
DATA SET READY	Pin 6
RECEIVED LINE SIGNAL DETECTOR	Pin 8

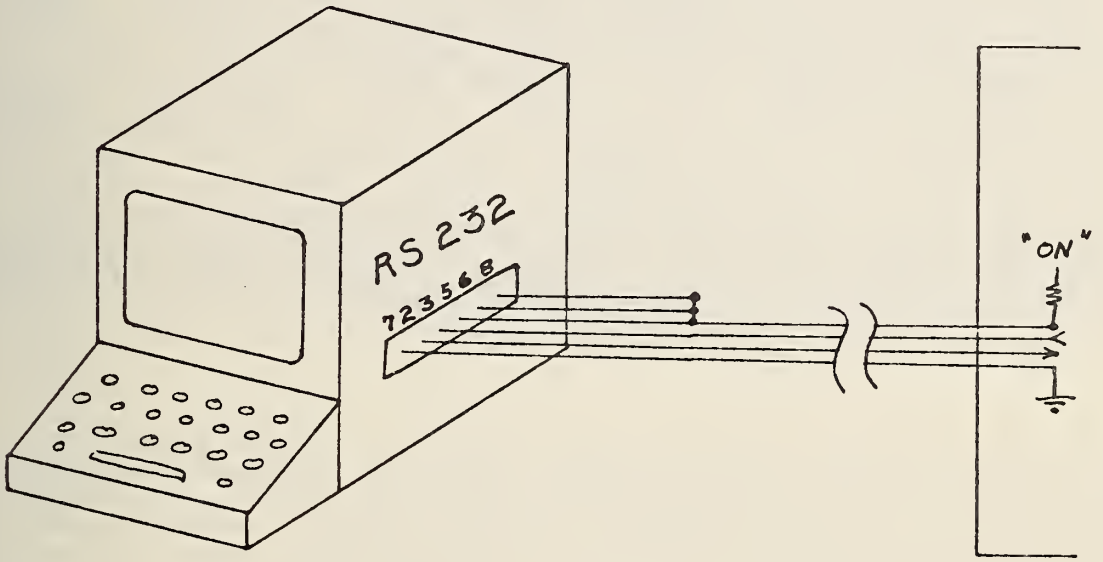


Figure 15

The first three are obvious for bidirectional communication and require no explanation. Their functions occupy three of the four wires in the cable. The remaining three functions represent control signals directed to the data terminal equipment. RS 232-C specifies that a DTE shall not transmit unless all three of these circuits are in the ON condition. These three circuits are all emergized by the fourth wire in the cable which is jumpered to pins 5, 6 and 8 at the RS 232-C connector of the data terminal. At the computer end of the cable this wire is maintained in the ON condition by a power supply. Thus the ON condition is seen by the data terminal equipment continuously on all three function pins.

Conclusions

Standardization of the DTE - DCE interface is of importance to the development of reliable, efficient and cost effective computer communications systems. Despite the fact that standards have been developed in the commercial sector, many problems still remain. As an example RS 232-C is not specified to operate over more than 12 meters of cable between DTE and DCE, as a result of the high driver impedance. Also the high impedance of both driver and receiver makes the circuit susceptible to pick-up of extraneous signals. The high voltages generate cross-talk in adjacent circuits, make shielding difficult, and create possible security problems. For these reasons RS 232-C has not been adopted by the American National Standards Institute.

The existence of standard interface specifications does not insure plug-to-plug interoperability of devices in all cases. Products of many data communications and computer peripheral manufacturers require specifically engineered interfaces. Often interface requirements vary from manufacturer to manufacturer, and vary often within one product line. EIA standards were originally designed around the Bell System 102 data set. Today this modem represents only a small part of the total interface equipment universe. Expanding requirements have added additional functions beyond those specified in the standards. Careful analysis of requirements in each individual DCE application is required, applicability of existing standards must be determined, additional requirements must be specified, and interface engineering efforts are required to provide needed capabilities. Alternatively, consideration can be given to newly developing DTE-DCE interface standards which are discussed under RS-449.

RS - 449

A new generation of interface standards has evolved to replace the well known and widely used RS 232-C which is limited by its inability to handle long cable runs and truly high data rates. These new standards include the common data terminal equipment to data communication equipment (DTE-DCE) interface for data transmission over analog telecommunication networks as well as direct DTE-DTE operation.

The first in the new series of data communications interface standards to be completed and approved are the general-purpose electrical characteristics for digital interface circuits. They are EIA Recommended Standards RS-422 for balanced circuits and RS-423 for unbalanced circuits. As such both form component parts of the RS-449 specification. The new standards were developed to meet the advancing state-of-the-art in integrated circuit technology and greatly enhance the performance, as compared to RS 232-C, of d.c. digital baseband signals across interfaces. It was necessary to develop two general-purpose standards, one for balanced and another for unbalanced electrical characteristics to provide a wide range of flexibility for user applications.

The balanced electrical characteristics of RS-422 are designed for applications using typical twisted-pair telephone cable. High quality signals can be provided over cable distances up to 1200 meters at data signalling rates up to 100 kbit/s while higher data signalling rates, up to 10 mbit/s, can be employed for cable distances progressively decreasing to 12 meters.

These operating distances, as specified in Section 7 of RS-422, were set as conservative guidelines to ensure reliable performance in a wide range of user environments. With additional consideration given to the specific application, however, greatly increased operating distances can be realized. While keeping within the environmental constraints specified in Section 5 of RS-422, the cable length becomes a function of the cable parameters, cable termination, and amount of signal distortion (jitter) that can be tolerated. It has been shown empirically that cable distances of several kilometers are possible for lower data signalling rates.

The greatly improved performance now available from the balanced electrical characteristics opens the way for a number of applications where data terminal equipment (DTE) can be directly connected via twisted pair cable to a central computer, concentrator or other DTE's within a large facility. As a result, the requirement and expense is eliminated for data communicating equipment (DCE), such as modems or data sets, for such "in-house" applications.

The unbalanced electrical characteristics of RS-423 are designed to provide superior performance to those of RS 232-C. A low impedance single-ended generator is specified with a differential receiver having a transition threshold of 200mV. Operation over cable distances up to 1200 meters at data signalling rates up to 3 kbit/s provide good quality signals while keeping near-end crosstalk within 1 volt peak. Likewise, higher data signalling rates up to 300 kbit/s can also be employed for cable distances progressively decreasing to 12 meters. The primary limitation of operating distance with unbalanced circuits is near-end crosstalk, rather than signal quality as with the balanced circuits. In comparison, the performance of RS 232-C is generally limited to cable distances of 15 meters at data signalling rates up to 20 kbit/s.

The most significant feature built into RS-423 is its capability to interoperate with both RS 232-C circuits and RS-422 circuits. This provides the key mechanism for an orderly transition from RS 232-C to the new generation of interface standards. The approach taken was to place the onus for interoperability on the equipment implementing RS-423, so that no retrofitting will be required for existing RS 232-C equipment. However, when interoperating with RS 232-C equipment, performance is limited to that associated with RS 232-C.

The unbalanced electrical characteristics allow a user to gracefully phase existing equipment out of use while bringing in a new generation of equipment to meet advancing requirements. At the same time, a signficant improvement in operating performance can be realized as the RS 232-C equipment phases out. As a separate stand-alone standards, RS-423 can be referenced for application by specific interface standards, as discussed later, as well as specified for any special purpose user application.

The DTE-DCE interface for applications involving modems has traditionally required the use of a number of parallel control circuits for operation of the modem. These are necessary for such functions as changing direction of transmission in half duplex operation over 2-wire circuits, modem synchronization and conrol of fault isolation loopback.

EIA RS-449 provides the complete transition mechanism with the objective of evolving to the future mechanism with the with the objective of evolving to the future generation of equipment. RS-449 has been primarily designed, as RS 232-C, for user applications which allows equipment of one manufacturer on one side of the interface to be directly connected to equipment of another manufacturer on the other side of the interface without additional technical considerations.

One of the more notable improvements of RS-449 over RS 232-C is the use of the new unbalanced electrical characteristics of RS-423. Not only does this provide significantly improved performance between RS-449 equipment, but facilitates interoperability with RS 232-C. The full potential performance of RS-423, however, has not been used to full advantage by RS-449 because of the requirement for compatibility with RS 232-C. Consequential design decisions limit the RS-449 equipment to data signalling rates of 60 kbit/s

and cable distances of 61 meters. This is still a significant improvement over RS 232-C which is limited to 20 kbit/s and 12 meters.

The second step in interface evolution is the provision for use of the balanced RS-422 electrical characteristics on the interchange circuits that may switch at the operating data signalling rate. These include data, timing, and selected control circuits. The option of being able to implement either the RS-423 or the RS-422 electrical characteristics on these circuits provides for full plug compatibility.

When the balanced RS-422 option if applied, operating into the Mbit/s range can be employed. As a result of the much wider range of operating characteristics that are possible, the necessity for additional technical considerations outside the scope of the standard to tailor specific applications is greatly reduced. The improved operation performance also makes DTE to DTE operation economicaly practical. Accordingly RS-449 also will include suitable direct connection configurations without intermediate DCE's which is an ideal configuration for use with the AES control system.

In summary, RS-449 offers considerable flexibility as well as signficantly improved performance to the user. When a transition must be made from existing RS 232-C equipment, the user would use RS-449 equipment implementing RS-423 unbalanced electrical characteristics on all circuits. The old equipment can then gradually phase out of use. Where a transition is not required, the user would implement RS-449 with the RS-422 balanced electrical characteristics on the selected circuits. This would provide superior performance and additional flexibility in the AES application.

IEEE 583 (CAMAC)

In 1975 the Institute of Electrical and Electronic Engineers (IEEE) published basic specifications for Computer Automated Measurement and Control (CAMAC). These specifications describe a complete modular instrumentation/interface system with all of the mechanical, electrical, and signal characteristics, as well as the protocol, fully defined to assure interchangeability and compatibility. Developed originally in the nuclear field, CAMAC has spread into a wide variety of industrial, laboratory and medical applications. CAMAC is a high speed instrumentation and interface system in which modular functional units connect to a standardized data highway (Dataway) for transmission of digital informtion. It is the only widely used nonproprietary interface system based on interchangeable standardized plug-in modules. Figure 16 gives a brief overview of a CAMAC system showing the various interfaces.

The modules, which are interchangeable regardless of source, plug into a standardized enclosure (crate) that includes the Datway along which the data and control information are carried. The Dataway is a parallel bus that can handle data words of up to 24 bits. Minimum Dataway cycle time is one microsecond. Each crate can accommodate up to 23 modules plus a crate controller. Since the modules are addressed by dedicated lines from the crate controller, they can be addressed individually or in multiple, in any combintaion. There are 16 subaddresses and 32 functions, binary coded. Thus the addressing capability is very high. Multiple crate systems can utilize a defined standardized parallel highway that can accommodate up to 7 crates per branch, a defined standardized serial highway that can accommodate up to 62 crates, or other types of highways, as may be desired. The system also has interrupt capabilities with demands lines from the modules to the crate controller.

Control applications where long distances are involved use serial highways to economize on cabling costs. The standardized CAMAC serial highway, which can be either bit serial or byte serial (8 bits per byte), has a maximum spped of up to 5 MHz though this drops as the number of crates and the line length is increased.

The basic CAMAC specifications, the CAMAC parallel and serial highways, and CAMAC block transfer conventions, are all IEEE standards as listed below. They are also international standards (adopted or in process) of the International Electrotechnical Commission.

1.	Basic CAMAC Specs	IEEE Std 583-1975	IEC 516
2.	CAMAC Serial Highway	IEEE Std 595-1976	In process at IEC
3.	CAMAC Parallel Highway	IEEE Std 596-1976	IEC 552
4.	CAMAC Block Transfer	IEEE Std 683-1976	In process at IEC

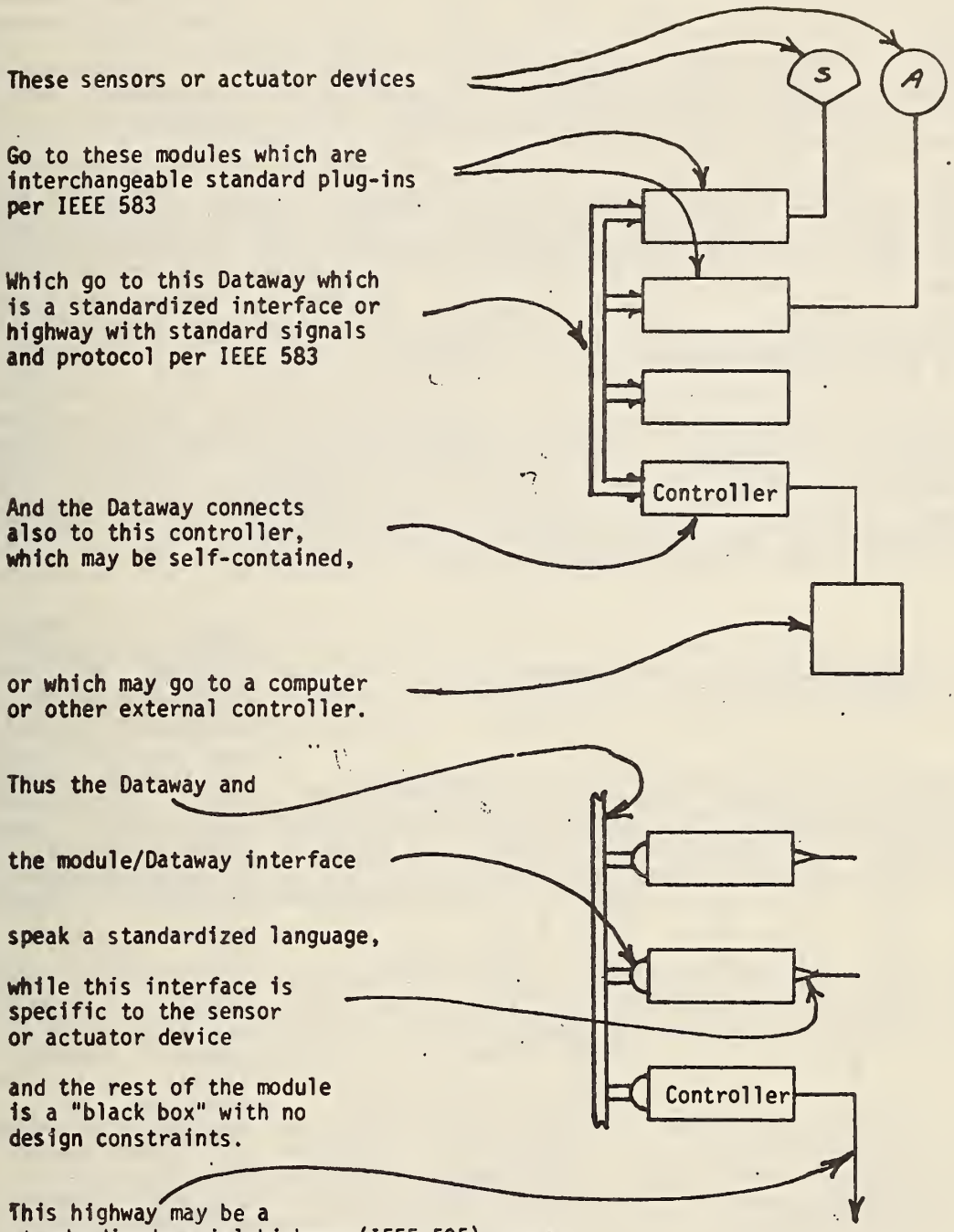

These sensors or actuator devices
S
A
Go to these modules which are interchangeable standard plug-ins per IEEE 583
Which go to this Dataway which is a standardized interface or highway with standard signals and protocol per IEEE 583
Controller
And the Dataway connects also to this controller, which may be self-contained,
or which may go to a computer or other external controller.
Thus the Dataway and
the module/Dataway interface
speak a standardized language,
while this interface is specific to the sensor or actuator device
Controller
and the rest of the module is a "black box" with no design constraints.
This highway may be a standardized serial highway (IEEE 595), or a standardized parallel highway (IEEE 596), or a non-standard highway.

Figure 16

Technical Description

Incompatible instruments have long been the rule in laboratories and industrial organizations The problems they pose are enormous and expensive. The concern is with interfaces, mechanical, electrical, and from a signal standpoint. Besides the inefficiency inherent in a multiplicity of different interfaces, the man hours of design effort is taggering, and this effort is needlessly repreated for installation after installation.

The CAMAC standard has been developed to alleviate these problems and is gaining wide international acceptance. The system features a fully specified data highway (Dataway) together with modular functional units that are completely compatible and that are available from diverse sources. Additional levels of compatibility are achieved through the use of standardized parallel and serival highways that have been developed for use with the basic CAMAC system.

Many installations exist in which various instruments are interfaced to each other and to a computer. Large numbers and large varieties of interfaces are involved. Though this uneconomical arrangement predates current technology, it is none the less in very widespread use. The money and effort expended on such interfacing is immense, and that is the problem that has been alleviated by the CAMAC system.

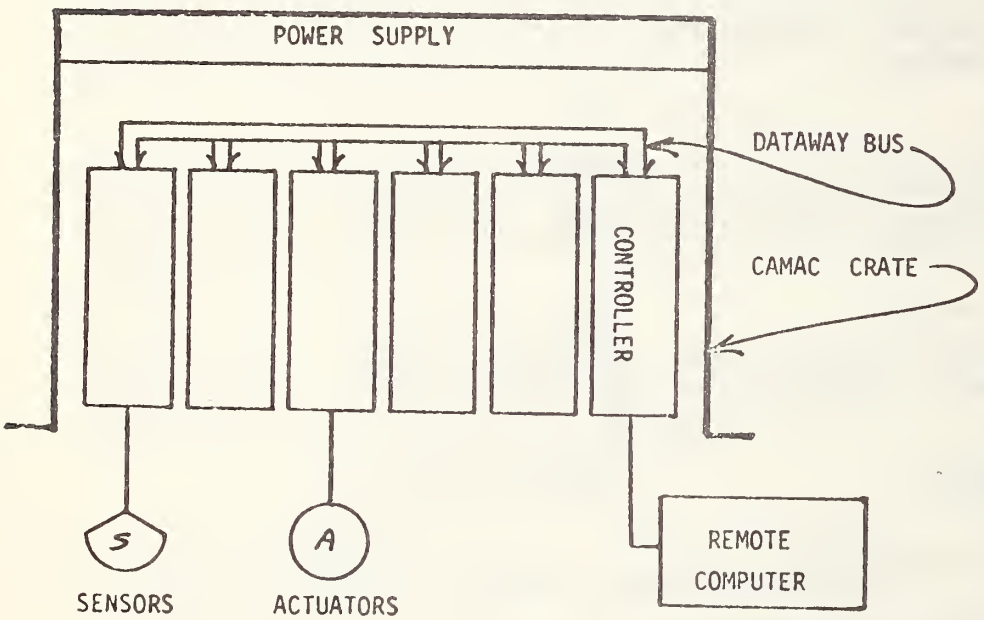


Figure 17

Figure 17 shows the CAMAC arrangement which involves standardization of the mechanical, electrical, and signal interfaces. The standardization of the mechanical and electrical interfaces permits installation of a multiplicity of modular instruments, of various designs and from diverse sources, in a common enclosure (or crate) and operating from a common power supply. The signal interface is provided by a bused "Dataway" at the rear of the crate with clearly spelled out signal standards and "rules of the road" for the Dataway and for the connections to the Dataway.

The figure also shows how sensors, actuators and peripherals communicate with the computer via CAMAC modules through the common Dataway and a single interface.

The system has a 1 microsecond Dataway cycle time and a very high addressing capability. The Dataway is parallel, with 24 read lines and 24 write lines, so that words of 24 bits or less can be handled in a single data transfer. Typically, up to 23 stations can be addressed within a crate, either singly or in any combination, with 16 subaddresses for each station together with 32 function codes. This high addressing capability is further multiplied by 7 in the case of the standard 7 crate parallel highway system and by 62 in the case of the standard serial highway system, both of which are discussed later.

CAMAC instruments are modular functional units that are accommodated in a CAMAC crate. A typical CAMAC module is based on the standard 222 mm high panel and has a basic single width of 17 mm . The modules can come in any multiple of this basic single width. The specifications allow complete flexibility with regard to the internal design of the modular instruments. The instrument is treated as a "black box" with the standardization confined to the external mechanical configuration, the electrical power requirements, and the signal inputs and outputs. This permits instrument compatibility and interchangeability without restricting the internal functioning of the instruments or the design details.

The CAMAC crate serves as the common housing for CAMAC instruments and also provides the Dataway for all the instruments that are inserted in the crate. The instruments receive digital inputs from and transmit their digital outputs along the Dataway.

All stations into which the modular instruments can be inserted are identical except for the control station which is located at the extreme right. This station is reserved for the crate controller which handles all communications between the instruments and the Dataway and also between the crates and the computer or other external controller.

A typical CAMAC crate can accommodate up to 25 single-width modules (though a minimum of two of these are required for the crate controller), or a lesser number of wider modules. Single width modules and modules of any multiple width can be inserted in any combination.

The Dataway at the rear of a CAMAC crate consists primarily of bused lines that interconnect the stations and that are utilized to transmit read, write, controls and addressing information. The Dataway includes also power supply buses as well as a limited number of dedicated lines. The controller addresses specific stations, singly or in any combination, by means of dedicated station lines. A second set of dedicated lines is used by the instruments to alert the controller when they want attention. This interrupt capability is an important feature of CAMAC that has proved to be of immense value. The Dataway consists of both buses and deciated lines.

In a 25 station crate, 24 are designated "normal" stations and are wired identically. The wiring of the control station is different from that of the normal stations. Since a crate controller must hav access to the Read R and Write W bus lines, it must occupy at least one normal station in addition to the control station.

The Dataway lines fall into four categories as follows:

1. All Station Bus Lines linking corresponding Dataway connector contacts at all stations, including the control station.

2. Normal Station Bus Lines linking corresponding Dataway connector contacts at all normal stations, but not connected to the control station. (These include the Read and Write lines.)

3. Individual Lines between the control station and each normal station. There are two such lines for each normal station:

    1. the N line (Station Number line) by which the control station addresses specific normal station, and

    2. the L line (Look-At-Me line) which is a demand line used by the station to advise the control station that it wishes attention.

4. Patch Contacts (for each station) that are not connected to the Dataway and are available for patch connections.

CAMAC systems vary from simple single-crate systems to complex and extensive systems with a vast number of crates distributed over a considerable area. The instruments within the crate all speak a common language to the Dataway. The controller, while also speaking the common Dataway language, serves as a translator if the crate is connected to a computer. The controller is then the one unit in the crate that must be able to communicate directly with the computer. Controllers of this sort, dedicated to specific computers, have been produced for a number of computers.

In many instances, it is advantageous to make even the crate controller computer independent. This is done by interposing a branch driver between the crate controller and the computer. The crate controller then speaks the Dataway language and a standardized highway language. The Branch Driver also speaks the highway language, but it assumes the role of dedicated translator and must speak also the computer language. A single branch driver, capable of serving a multiplicity of crates, now becomes the one computer dependent device in the installation.

The interconnection between crates and between the crates and a computer or other controller is called the Highway. With dedicated crate controllers

designed to interface with specific computers, the Highway becomes an extension of the computer I/O bus. Where branch drivers are used, that portion of the Highway that interconnects the crates and branch driver can be computer independent. Such highways can be either parallel or serial, single-ended or balanced.

Parallel highways are inherently capable of the highest data transfer rate and have maximum transparency to the Dataway. They are especially attractive where the highway length is not excessive so that a single-ended highway can be used [see A2.1 of IEEE Std 596-1976, Parallel Highway Interface System (CAMAC)]. Parallel highways of greater length are feasible but this requires a balanced transmission mode, using either balanced transmitters and receivers or balanced-to-single-ended converters. Such converters permit use of single ended operation at the crates with balanced transmission over long-span portions of the highway. The standardized CAMAC parallel highway of IEEE Std 596-1976 using branch drivers and well defined crate controllers is in widespread use. The crate controllers are available from a number of sources, and branch drivers are available for a wide variety of computers.

Serial highways using a limited number of lines are particularly attractive for installations where very long highways are required and where the highway wiring cost can be considerable significance. The standardized CAMAC Serial System of IEEE Std 595 is capable of handling up to 62 CAMAC crates. This serial system can be either bit serial or byte serial with 8 bits per byte.

The serial highway is interfaced to the computer through a serial driver or, where an unsophisticated interface of limited capability is acceptable, through an adaptor to the teletypewriter port of the computer. The highway is organized in a loop that begins at the defined output port of the serial driver, goes through a serial crate controller in each CAMAC crate, and then returns to the defined input port of the serial driver. The serial driver communicates with the computer through a port that is specific to the computer.

The capability of CAMAC systems can be further enhanced by the use of microprocessors within the modules. This permits "local" processing and thus reduces the load on the Dataway. Alternatively, the conventional crate controller ca be replaced or supplemented by microprocessor-type controllers that can reduce the load on the computer or even eliminate the need for a computer.

Non-CAMAC devices can be connected into CAMAC systems either in the highway or via the Dataway by means of an interfacing module. The measuring instrument interface bus of IEEE Std 488-1975, Digital Interface for Programmable Instrumentation and Related System Components (ANSI MC1.1-1975), can be connected to the CAMAC Dataway of IEEE Std 583-1975, by means of a simple interface module.

For added processing capability, the interface module can be of the microprocessor type such as has been designed and operated at the Los Alamos Scientific Laboratory. Various console control devices (encoders, keyboards, displays, etc) that use the IEEE Std 488-1975, digital interface bus are connected into a CAMAC system by means of this "intelligent" interface module.

CAMAC is a user-developed system which permits the configuration of installations that can be easily upgraded with time and which can be made practically independent of the control computer except for small sections of hardware and software. Updating of installations, such as industrial control systems, has traditionally been very difficult. Since these difficulties are not present in CAMAC systems with standardized multisource functional units, economical modernizing of CAMAC industrial control systems is feasible.

References

The four IEEE CAMAC standards have been compiled into a hard cover book published by IEEE and distributed in cooperation with John Wiley and Sons. This volume is identified as IEEE SH06437, Library of Congress Catalog No. 76-39660.

ERDA Report TID-26618 (October 1976) is a compilation of tutorial articles describing CAMAC. A great deal of information has also appeared in the literature. The ERDA report pages 7 and 8 contain an excellent reference list of articles and papers.

Mining applications would have a great deal in common with industrial control applications in harsh environments and therefore existing CAMAC industrial installations should be studied.

IEEE 488

In 1975, the Institute of Electrical and Electronic Engineers (IEEE) published the specifications for a Standard Digital Interface for Programmable Instrumentation (IEEE 488). In the same year the American National Standards Institute adopted the standard as ANSI MC 1.1-1975. The International Electrotechnical Commission is now in the process of approving the same document, with perhaps a few extensions, as an IEC standard.

IEEE 488 defines an interface that allows a user to interconnect various instrumentation with the assurance that messages and data can be accurately communicated within the system. The standard is rapidly becomming the most popular method for configuring several closely spaced but separate devices around a computer based controller. A wide variety of manufacturers are offering analog as well as digital equipment with the 488 interface, and the trend is growing. One US instrument house estimates that while only 10 % of their 1975 shipments were equipped with the IEEE 488, the figure jumped to 30 - 50 % in 1976. A German firm reported half of their sales in 1976 were bus compatible, and a French expert estimated 20 % of the French instrumentation market desired the 488 compatibility.

The mechanical, electrical and functional characteristics of the interface are completely specified leaving the implementors free to choose the character coding and protocol for any data transmission.

Technical Description

The IEEE 488 bus scheme allows separately manufactured devices to be interconnected to act as an integrated instrumentation system. Figure 18 illustrates this configuration and shows the three functions being performed: listener, talker and controller. It should be noted that any or all of these functions can reside in a single device. That is, a counter is usually just a talker, but a multimeter is both talker and listener. Furthermore, a microcomputer could incorporate all three functions. The only limitation is that there be only one controller.

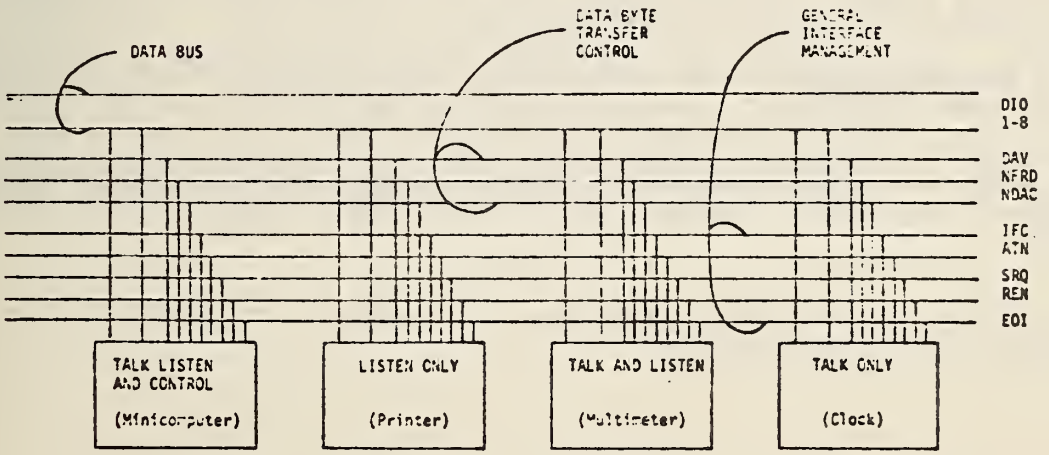


Figure 18

As many as 14 devices can listen and receive data at any one time. The bus control lines will insure that even the solwest of the devices will be serviced without loss of data. Thus the standard appears to offer many advantages to a user wanting to piece together a variety of stand alone devices from different manufacturers into a specific instrumentation system without a great deal of special engineering.

The data bus which connects these components is comprised of sixteen signal lines. The physical bus itself is a length of cable with the standardized, stackable connectors at each end. The standard allows 2 meters of cable per instrument or 20 meters total. In this respect IEEE 488 differs from other parallel bus schemes which involve backplane wiring in a single chassis. No power leads are carried in the 488 bus. Each interconnected instrument supplies its own power.

Of the 16 lines comprising the bus 8 are used for bidirectional data transmission, 3 for the control of the data lines and 5 for general interface management.

A data bus of eight interface signal lines carries all 7 bit data.

(1) DIO1 (data input output 1)
(2) DIO2 (data input output 2)
(3)
-
-
(8) DIO8 (data input output 8)

Data are carried on the DIO signal lines in a bit-parallel byte-serial form, asynchronously, and generally in a bidirectional manner.

A set of three interface signal lines is used to effect the transfer of each byte of data on the DIO signal lines from an addressed talker to all addressed listeners:

1. DAV(data valid) is used to indicate the condition (availability and validity) of information on the DIO signal lines.

2. NRFD (not ready for data) is used to indicate the condition of readiness of device(s) to accept data.

3. NDAC (no data accepted) is used to indicate the condition of acceptance of data by device(s).

The DAV, NRFD, and NDAC signal lines operate in what is called a three-wire (interlocked) handshake process to transfer each data byte across the interface.

Five interface signal lines are used to manage an orderly flow of information across the interface:

1. ATN (attention) is used to specify how data on the DIO signal lines are to be interpreted and which devices must respond to the data.

2. IFC (interface clear) is used to place the interface system in a known quiescent state.

3. SRQ (service request) is used by a device to indicate the need for attention and to request an interruption of the current sequence of events.

4. REN (remote enable) is used in conjunction with other messages to select between two alternate sources of device programming data.

5. EOI (end or identify) is used to indicate the end of a multiple byte transfer sequence or, in conjunction with ATN, to execute a polling sequence.

For data to be transmitted over the bus it is necessary for the controller to designate the talker from which the data is to come and the listner or listners where the data is to go. The DIO lines carry all the data while the other 8 lines control the flow and interpretation of that data. The data can be actual measurement data, program data, addresses or commands. The type of data is indicated by the ATN line. With ATN true the data is either addresses or commands and all devices are expected to pay attention; with ATN false the data represents measurement or program data being transferred between a previsouly addressed talker and listner.

The actual transfer of a single data byte on the DIO lines is controlled by the DAV, NRFD and NDAC lines. DAV is sent by the talker to all listeners to indicate that the data is ready for transfer. NRFD is used by listeners to indicate their readiness to accept data, and NDAC signals that the listener has accepted the data. A typical transfer starts with DAV high. On seeing this all listeners set NRFD low showing they are not yet ready to receive and NDAC low showing they have not accepted the data. Seeing both signals low the talker puts the data onto the DIO lines. When NRFD goes high indicating all listeners are ready, the talker sets DAV low to initiate the data transfer. Each listener sets NRFD low and begins to accept the data. When completed it sets NDAC high. Sine the line is wire-ored, it will not go high until all listeners have accepted the data. When NDAC does go high, the talker knows everyone has received the data. Talker then sets DAV high and clears the DIO lines placing the system back into its initial state. Thus the system is asynchronous and device speed independent, accommodating both the fastest and the slowest of listeners and talkers.

Typical Application

The configuration in Figure 19 has been designed to select a specific analog channel, digitize the signal, process the data, and print the result. Additionally, the system sounds an alarm if any data exceeds a specified limit. One complete cycle would involve the following exchange:

1. Controller sends the listen address to the analog multiplexer followed by the channel address to be digitized and the unlisten command.
2. Controller sends the listen address to the A/D converter followed by the program code required to initiate a measurement and the unlisten command.
3. Controller addresses itself to listen then sends the talk address to the A/D converter thus initiating the data transfer.
4. Controller receives the data, processes it and sends the unlisten command.
5. If data are within proper range, the controller addresses the printer to listen and the controller to talk.
6. If any data are over range, the controller addresses the alarm to listen and itself to talk. It then sends the proper program code to the alarm to indicate the data are out of range.

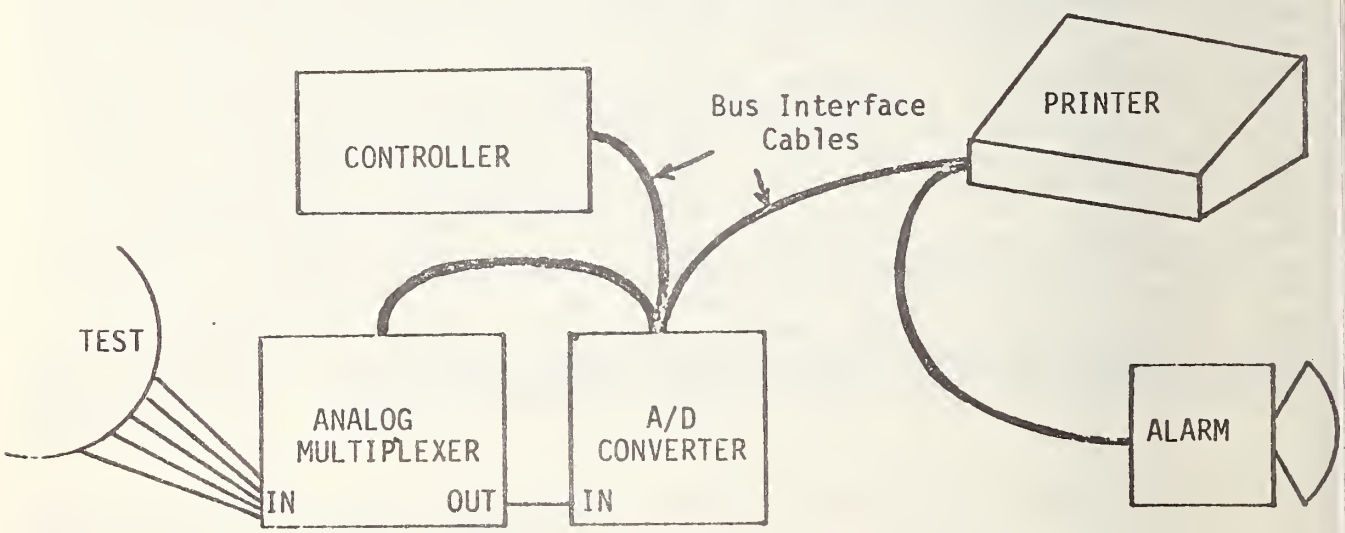


Figure 19

Conclusions

IEEE 488 describes a bus scheme for interfacing a variety of separate instruments into an integrated system without special engineering. It is widely used and readily available from numerous suppliers. The popularity of IEEE 488 appears to be increasing. To summarize, the standard applies to systems in which:

1. Only digital data is to be exchanged across the bus.
2. As few as two and up to fifteen devices are to be connected.
3. Maximum length of the bus is 20 meters.
4. Maximum data rate across the bus is one million bits per second.

Some users report that the maximum data rate across the bus is too low for some applications. Others find difficulty in that the standard does not specify the character code to be used for data bytes. This has led to different manufacturers adopting their own (ASCII, BCD, etc) thus causing problems for users of that equipment.

An additional area of concern is that the extra cost for providing an instrument with the optional interface to 488. One manufacturer has estimated that the standard adds from $50 to $900 to the cost of an instrument depending on the range of functions needed. This cost will decrease as special LSI chips are developed. One chip acting as a receiver-transmitter is already available to interface with the bus electrically but provides none of the logic functions needed.

Dispite these potential problems IEEE 488 is finding much use as a solution to many common problems of instrumentation systems.

MILSTD 1553 A

INTRODUCTION

In 1975, the US Department of Defense published basic specifications for an aircraft multiplex Data Bus (MIL-STD-1553A). These specifications describe a complete modular instrumentation interface with all of the electrical and signal characteristics, as well as the protocol, fully defined to assure compatibility. MIL-STD-1553A was developed expressly for avionics systems but may find applicability in other vehicle control systems. It is a high speed instrumentation and interface system in which modular functional units (Remote Terminals or "RTs") connect to a standardized Data Bus for transmission of digital information.

The RTs, which may be supplied by any manufacturer, attach to the Data Bus through a specified RT/Bus interface as in Figure 20. The Data Bus itself is a serial bus that handles words with 16 bits of data, a sync waveform, and a parity bit for a total of 20 bits per word. The Data Bus cycle time is 1.0 microseconds. The Bus can handle up to 32 RTs. The RT can recognize its address and accept messages directed to it which may be in the form of data, control, or status words. The manufacturer may design the RT/Bus interface into the subsystem or build it as a separate module. In the management of the F-16, General Dynamics specified that the manufacturers of avionics subsystems build the interface into the deliverable subsystem so that standalone acceptance tests could be conducted.

It is intended that this standard be used to facilitate the system design process. For this reason, the standard is deliberately vague concerning the use of redundancy in implementing the Bus system. The use of redundancy, the degree to which redundancy is necessary to increase reliability, and the form it takes are not included in this standard. However, the application of this standard to the F-18 makes use of redundant Data Buses as well as redundant Bus Controllers as needed by the system designer.

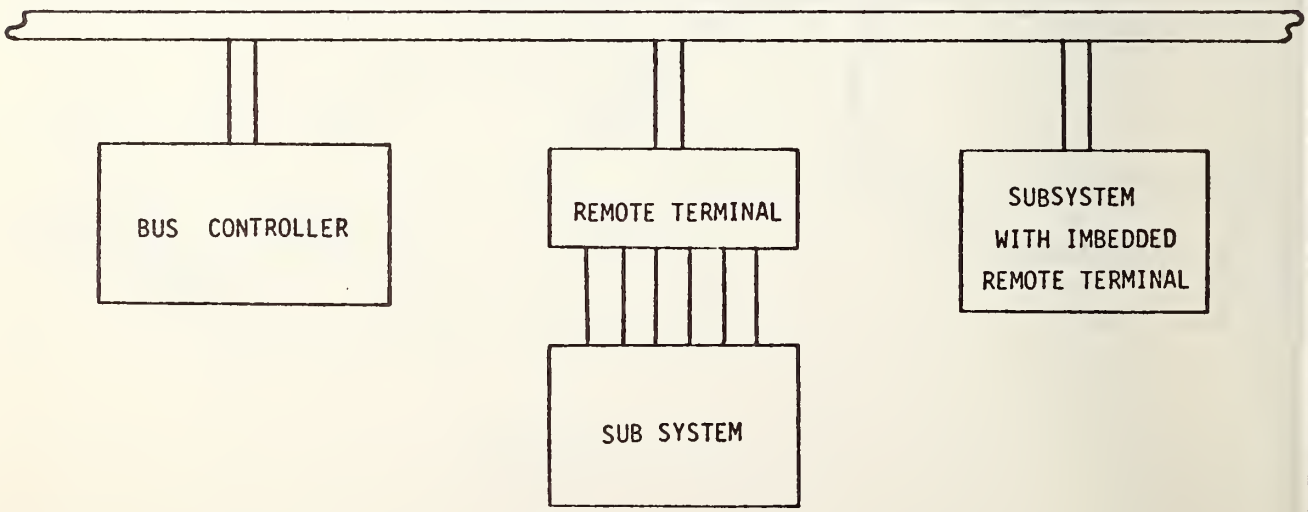


Figure 20

At the present time this standard is being applied to the F-16, F-18 and the Army Advanced Armed Helicopter. All of these avionics systems have been custom built by avionics manufacturers who are interested in providing the complete system as a package. For this reason, it is an expensive system to install at the present time. The Air Force is funding an effort to build RT interfaces using LSI technology to reduce costs, but no product is expected until 1979.

Technical Description

This bus is designed to operate in a command/response mode so that the Bus controller initiates all message transfers. Three types of message transfers are possible: controller to RT, RT to controller, and RT to RT. Even though this Bus could be called a "distributed communication network" since it permits RT to RT transfers, full hierarchical control of the system is maintained by the Bus controller. For example, in the controller to RT transfer, the controller sends a "receive" command followed by the specified number of data words. The RT, after validating the message, transmits a status word back to the controller. In an RT to controller transfer, the controller issues a "transmit" command to the RT, and the RT responds by returning a status word and the specified number of data words. Lastly, in an RT to RT transfer, the controller issues a receive command to RTA, followed by a transmit command RTB. Upon completion, RTB returns a status word back to the controller.

The transmission facility is a two conductor, twisted shielded cable with a characteristic impedance of 70 ohms. The cable length of the main Bus may be up to 92 meters.

The remote terminal (RT) is the unit that electronically interface the Bus with the subsystems and the subsystems with the Bus. It may be a separate unit to which the subsystem interfaces, or may be imbedded in the subsystem. A redundant bus controller, when not functioning as a controller, may operate as a remote terminal.

The Bus controller is a key part of the Data Bus system. It is responsible for sending Data Bus commands, participating in data transfer, receiving status responses, and monitoring system status. It is assumed that most of the routine minute details of bus monitoring (e.g. parity checking, terminal non-response checkout, etc.) will be accomplished by hardware, while the algorithms for bus control and decus bus control and decision making will reside in software. The controller can be either a standalone computer dedicated to bus management or a peripheral I/O controlled on an existing central computer.

Typical Application

Figure 21 is a schematic of the avionics multiplex system associated with the F-18 aircraft. Two digital computer will function as Bus controllers. In this redundant system, either computer can act as Bus controller if one should fail. Also, each can communicate with every avionics subsystem through redundant Buses.

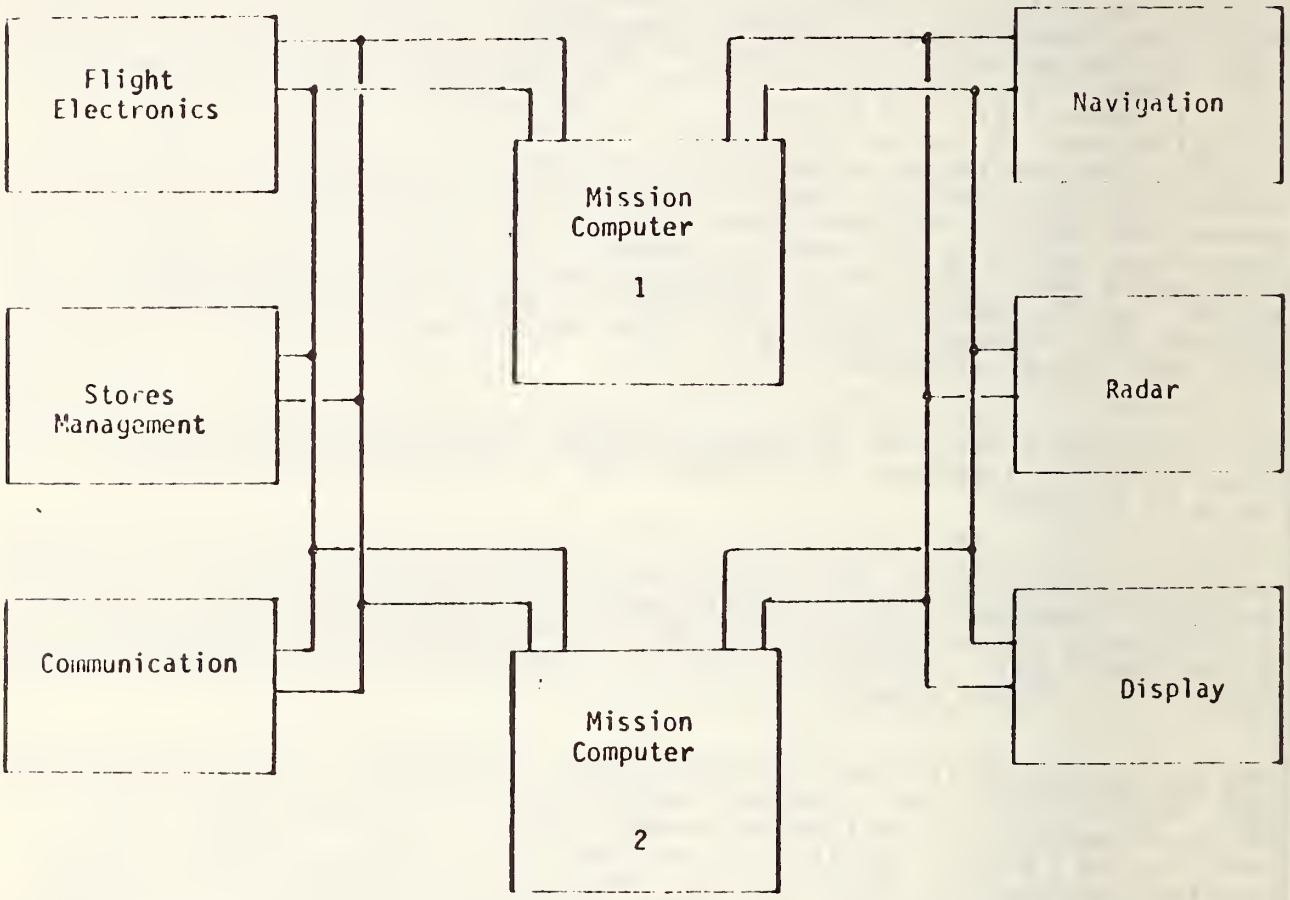


Figure 21

References

1. MIL-STD-1553A "Aircraft Internal Time Division Command/Response Multiplex Data Bus," 30 April, 1975.

2. "Avionics: Military Moves to Multiplex for Aircraft," Aviation Week and Space Technology, Nov.29, 1976, p. 56.

3. "Avionics: Navy Pushing Microprocessor Utilization," Aviation Week and Space Technology, Aug. 11, 1975, p. 48.

ANSI X3.28-1976

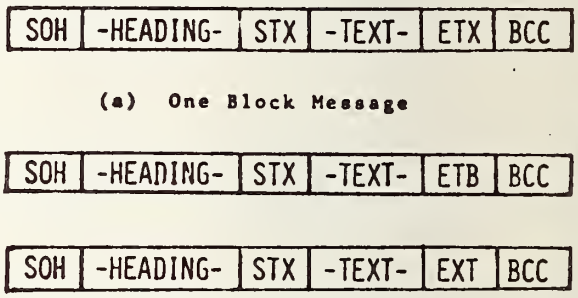
The procedures of American National Standard X3.28-1976 treat the bit stream of a digital serial communications link as a sequence of characters. The standard utilizes the ten communications control characters (hereafter called control characters) of the ASCII (ANSI X3.4) character set to define link control and specify procedures for establishing, using and terminating a link connection.

A problem with X3.28 is that, rather than giving a coherent solution to the problem of link control, the standard is essentially a list of approved alternative solutions.

Ten subcategories of establishment/termination procedures are specified and fourteen subcategories of message transfer procedures. Thus, there are 140 possible systems which are standardized by X3.28. However, only about 80 of these can actually be realized, and most of these systems are incompatible with each other. In X3.28, link configuration is included in the definition of the procedures for establishing and terminating a connection on the link.

Framing

The message is "framed" by certain control characters as indicated in Figure 22. Every block begins with a start of heading (SOH) if a header is present or a start of text (STX) otherwise. If the message is multi-block, the blocks other than the last are terminated by an end of block (ETB). The last block of a message (including the one-block message) is terminated by an end of text (ETX).



(a) One Block Message

(b) Multi-Block Message

Figure 22

Data communications under X3.28 consists of the transmission of character streams from one terminal to another. The primary purpose of the procedures described below is to facilitate the sending of "information messages" (or messages, for short) which are strings of characters of user data. Some of the subcategories require that no control characters appear anywhere in these strings of data, while other subcategories provide for transparent operation by prefixing each meaningful control character within the text of a message with a Data Link Escape character (DLE) and by "doubling" DLE's. The receiver removes these extra DLE's.

Messages in X3.28 are otherwise unspecified as to content or length. However, for purposes of efficiency or convenience, the implementor may, depending on the procedure chosen, split a message into "blocks," each one of which is transmitted separately, with reassembly at the receiving terminal. A message or block may be further divided into two sections, transmitted together, called the header and the text. No specification of form or content for either section is provided in the standard.

Note that the standard does not dictate the means by which blocks are correctly reassembled into a message. However, the blocks are serially transmitted in proper sequency. In general, decisions on blocking are left to the implementor. The only constraint made by the standard is that of the individual subcategories to support no blocking, message associated, or message independent blocking.

Control Procedures

Table 4 lists the control characters to be used for link control, as well as the character sequences extending the basic set. There are several classes of messages, as dictated by the control characters framing the message. The actual interpretation of the characters is discussed with the procedures specific to each category.

CHARACTER	MEANING
SOH	Start of heading
STX	Start of text
ETX	End of text
EOT	End of transmission
ETB	End of block
ENQ	Enquire (request for response)
ACK	Positive acknowledge
NAK	Negative acknowledge
SYN	Synchronous idle
DLE	Data link escape
DEOT	Mandatory disconnect (DLE,EOT)
ACKO	Alternate Acknowledge 0 (DLE,0)
ACKL	Alternate Acknowledge 1 (DLE,1)

Table 4 - ASCII Communications Control Characters

The link supports three kinds of messages, forward supervisory, backward supervisory, and information. The forward supervisory message is initiated by the master station; its main purpose is to transmit control information rather than data. The backward supervisory message is initiated by a slave in response to a transmission from a master station. The information message carries otherwise unstructured data and is initiated by the master station. In general, it is expected that between any two (noncontiguous) blocks there will be (at least) two SYN characters transmitted to maintain synchronization of the two stations.

The control procedures in X3.28 are divided into two types of subcategories, establishment and termination and message transfer. The "definition" of a data link requires one procedure subcategory from each class.

Figure 23 depicts the general case of data transmission, broken down into phases. Phases 1 and 5, not shown here, are circuit connect and disconnect respectively (applicable only to circuit-switched networks). They are not governed by the standard although they appear in the state diagrams of the

X3.28 document. Phase 2 is establishment, phase 3 is message transfer, and phase 4 is termination. The discussion of establishment and termination procedures below is in terms of the link subcategories above.

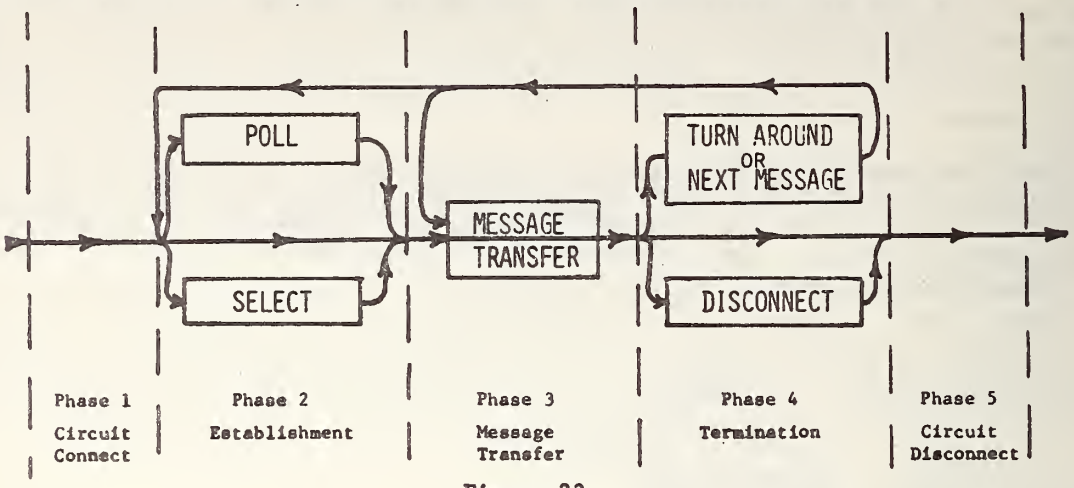


Figure 23

Establishment and Termination Subcategories

Phases 2 and 4 of transmission, described by procedure subcategory, are concerned with selection, polling, contention, line turn-around, and link disconnect.

Message Transfer Subcategories

These procedures cover the transmission of information messages (i.e., phase 3 transmissions) and the valid responses to them. As mentioned earlier, not all combinations of establishment and termination subcategories and message transfer subcategories make sense or can be realized. A designer should consult the standard for details.

Error Detection

In some procedures (A2,B2,B2) X3.28 provides for error detection beyond character parity by means of longitudinal redundancy checking (LRC: exclusive OR of each bit position) to provide a block-check character (BCC). This character is transmitted immediately following the ETB or ETX of an information message. As indicated earlier in Figure 22, the characters following the first SOH or STX (including STX if SOH is used) and including the ETB or ETX, are included in the computation of BCC. Any internal SYN's are excluded.

Certain subcategories provide for more sophisticated error checking in the form of cyclic redundancy checking for the subcategory providing transparent operation. Either the CCITT polynomial or IBM's CRC-16 polynomial may be used in computing the cyclic redundancy check.

ANSI ADCCP

Bit oriented procedures have been advanced both because of their inherently higher efficiency (in terms of line utilization) and as a way to "start fresh" from the maze of different configurations in X3.28. Until recently, these procedures were limited due to the computational complexity of framing, "bit-stuffing" and CRC computation, but the new microprocessor technology has opened the way for the widespread application of this type of procedure.

The American National Standards Institute is currently developing a proposed standard (X3S3.4/589, draft 6, Oct. 15, 1976) called Advanced Data Communication Control Procedures (ADCCP) which approaches the same problem as X3.28-1976, where different types of "messages" have different forms (e.g., selection vs. text transfer). The control characters are replaced by a subfield of the ADCCP frame which contains commands or responses to commands. Stations are identified by another subfield of the frame.

Link Configurations.

In ADCCP a terminal (or station) is permanently designated as being either Primary or Secondary. The Primary station is the control station of the link and has permanent master status. This might correspond to the AES systems controller should the systems designer choose to use a digital serial communications link. Similarly, the Secondary is in permanent slave status as could be all of the AES functional controllers.

The Primary station has the responsibility for link initialization, control and organization of data flow, and control of error recovery procedures at the link level, including retransmission. The Secondary has the responsibility to act only on the commands from the Primary, as described below.

ADCCP supports two general link configurations termed Primary/Primary and Primary/Secondary. The Primary/Primary link shown in Figure 24 is referred to as a balanced point-to-point link and consists in reality of two sublinks, each station comprising both a primary and a secondary component.

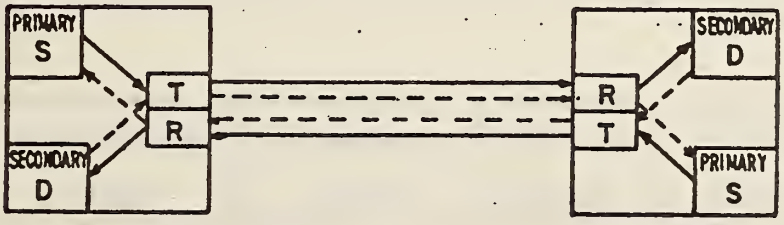


Figure 24

The Primary/Secondary link in Figure 25 consists of one primary station and one or more secondary stations. It may be characterized as two-way simultaneous or alternate, multipoint, and may be either switched or non-switched.

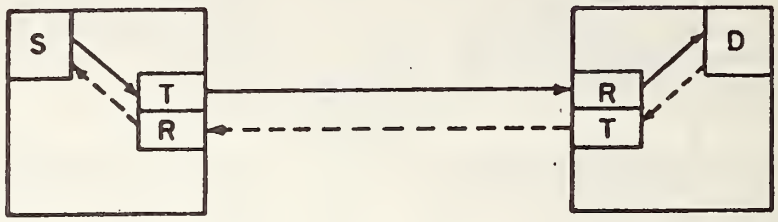


Figure 25

For an ADCCP link operating on a switched network, the called station, by convention, initiates transmission.

Note that all links in X3.28 can be accommodated, and the bewildering array of configurations have been replaced by just the two in ADCCP. The variety of message formats of X3.28 has been replaced by one (see framing, below) which presumably simplifies the link at both ends. Finally, the internal structure of a terminal has been extensively specified, thereby easing the burden of the implementor and hopefully minimizing the problems associated with modifying or extending the communications systems.

Framing

The unit of transmission in ADCCP is a frame, and all transmissions on the link utilize this format. The structure of a frame is shown below.

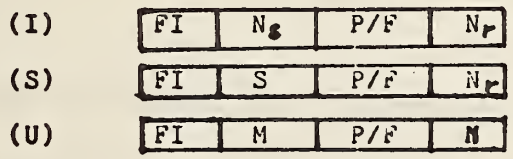
FLAG	ADDRESS FIELD	CONTROL FIELD	INFORMATION FIELD	FRAME CHECK FIELD	FLAG

Within a frame the fields are as follows.

Flag: An 8-bit sequency, 01111110, which begins and ends a frame. All terminals hunt for the flag in idle state, since this field is used for frame synchronization.

Address Field: An 8-bit sequency identifies a secondary terminal on the link. It may be extended (recursively) to provide for multiple octets. The structure is:

Control Field: Depending on the operational mode, the control field is one octet, extendible to two octets to allow for a larger range of sequence numbers. Note that the bit pattern for a command may be the same as that for a response, so that a knowledge of direction is necessary to interpret a frame. The control field has three formats; the I format containing the send and receive sequence numbers that is used for the exchange of data; the S format containing only receive sequency numbers that is used for conveying status and other sequentially dependent link control information; and the U format that does not contain sequence numbers and is used for other control functions such as setting modes or describing abnormal link conditions. These formats are summarized as follows:



The FI Field, common to all, dictates the interpretation of the remaining fields. It has three values, indicating an information transfer (I), supervisory (S), or unnumbered (U) frame. In the first case, the remaining fields are:

N_s : Send Sequence Number

P/F : Poll Command (from primary)
Last Frame Flag (from secondary)

N_r : Receive Sequence Number

A supervisory frame has fields P/F and N as above, and also an S field, which is used to inhibit the transmission of information fields in response frames, request retransmission of frames, or acknowledge the receipt of frames (when transmitted by a Primary) and to indicate a wait state, or acknowledge or request retransmission of information frames (when transmitted by a Secondary). A non-sequenced frame, containing no sequence numbers, has a P/F field as above and "modifier" fields, M, which are used to effect control of the link without changing sequence number counts.

In this scheme, a Primary-Secondary pair maintains a pair of sequency number counts, one for frames sent and one for frames received. The counts are dual in the sense that the send count for one station should agree with the receive count for the other.

Information Field: A field of length 0 or more bits. The maximum length is unspecified, as is its structure. In particular, it is completely transparent (i.e., code and byte independent), since addressing and commands are positional.

To achieve the transparency mentioned above, a process of bit-stuffing is used to assure that the flag sequence (01111110) does not appear within a frame. This is because a terminal must always check for the flag, either to terminate a frame or to maintain synchronization with other stations. A transmitting station must insert a 0 following five consecutive 1's, and a receiving station must remove it. (The receiving station examines the bit following five consecutive ones; if it is a zero it removes it).

Frame Check Sequency: A 16-bit Cyclic Redundancy Check (CRC) polynomial

$$X^{16} + X^{12} + X^{5} + 1$$

This field is computed on the basis of the contents of the address, control, and information fields.

Time-fill between frames is achieved by sending continuous flags or abort sequences. No provision is made for time-fill during frame transmission.

Address and Control fields are sent low-order bit first, the Frame Check Sequency is sent high-order bit first. Bit-sequencing for the Information field is applcation-dependent, and is unspecified.

A frame is considered invalid if it is not properly bounded between flags or if it is shorter than the minimum length of 32 bits (exclusive of flags). This allows for an address, control, and frame check sequence with a zero-length information field. Any invalid frame is merely ignored by the receiving station.

Error Detection

ADCCP provides the 16-bit CRC for detecting errors in transmission. In addition, a Response Timer is specified for the Primary, to detect no response from the Secondary. The sequential numbering scheme also helps detect lost or duplicated frames. An Abort sequence is provided (1111111) which allows a transmitting station to terminate transmission abnormally. The receiving station is expected to ignore an aborted frame.

Error Recovery

No provisions for recovery other than retransmission are made. The negative acknowledgements allow the Primary to decide whether retransmission will correct an error (short-term vs. long-term, and Link level vs. Higher level).

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This report describes interface standards applicable to the use of computer control systems with automated mining equipment. The report identifies, analyzes, and recommends interface standards applicable to the modular control system of an Automated Extraction System (AES) being built by the US Bureau of Mines (USBM). The work serves both as a technical guide and as a summary of existing and forthcoming standards applicable to computer control systems.

Since the system configuration of the AES control system has not yet been defined, this report uses several alternative architectures to illustrate various interfaces that may be encountered. The benefits and limitations of the formal and de facto standards which apply to these interfaces are then discussed. In this context, standards are recommended for the supervisory computer - local control computer interfaces and the local control computer - sensor and actuator interfaces. The best use of these standards and important trade-offs are identified and explained.

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